

Service Manual

LG-A258

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1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.

The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc. Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated by the sign. Following information is ESD handling:



- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current – Constant Voltage
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milli watt
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPB	General Purpose Interface Bus
GSM	Global System for Mobile Communications
IPUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop

1. INTRODUCTION

PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
PSRAM	Pseudo SRAM
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. PERFORMANCE

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Lithium-ion r, 3.7V, 900mAh	
Stand by TIME	Up to 290 hrs (Paging Period 5, RSSI -85dBm)	
Talk time	Up to 361min : GSM Tx Level 7	
Charging time	Approx. 3 hours	
RX Sensitivity	GSM, EGSM: -109dBm, DCS: -109dBm	
TX output power	GSM, EGSM: 33dBm(Level 5), DCS , PCS: 30dBm(Level 0)	
GPRS compatibility	Class 12	
SIM card type	3V Small	
Display	MAIN : 2.2" TFT 176 × 220 pixel 262K Color Sub : 0.968 mono 96 x 64	
Status Indicator	Button (Outside) Send Key, End Key, Navi Key(4EA), OK Key, Menu Key, Contacts Key Button (Inside) Numeric Key 12EA	
ANT	Internal	
EAR Phone Jack	5PIN I/O	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR/AMR	
Data and Fax	Yes	
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	
Microphone	Yes	

2. PERFORMANCE

Item	Feature	Comment
Speaker/Receiver	18x12Φ Speaker/ Receiver	
Travel Adapter	Yes	
MIDI	SW MIDI (Mono SPK)	
Camera	1.3M	
Bluetooth / FM Radio	Bluetooth version 2.1 / 76~108MHz supported	

2.2 Technical Specification

Item	Description	Specification					
1	Frequency Band	<div> EGSM TX: 880 ~ 915MHz RX: 925 ~ 960 MHz </div> <div> GSM850 TX: 824 ~ 849 MHz RX: 869 ~ 894 MHz </div> <div> DCS TX: 1710 ~ 1785 MHz RX: 1805 ~ 1880 MHz </div> <div> PCS TX: 1850 ~ 1910 MHz RX: 1930 ~ 1990 MHz </div>					
2	Phase Error	RMS < 5 degrees Peak < 20 degrees					
3	Frequency Error	< 0.1 ppm					
4	Power Level	GSM850 / EGSM					
		Level	Power	Toler.	Level	Power	Toler.
		5	33dBm	±2dB	13	17dBm	± 3dB
		6	31dBm	±3dB	14	15dBm	± 3dB
		7	29dBm	±3dB	15	13dBm	± 3dB
		8	27dBm	±3dB	16	11dBm	± 5dB
		9	25dBm	±3dB	17	9dBm	± 5dB
		10	23dBm	±3dB	18	7dBm	± 5dB
		11	21dBm	±3dB	19	5dBm	± 5dB
		12	19dBm	±3dB			
		DCS/PCS					
		Level	Power	Toler.	Level	Power	Toler.
		0	30dBm	±2dB	8	14dBm	± 3dB
		1	28dBm	±3dB	9	12dBm	± 4dB
		2	26dBm	±3dB	10	10dBm	± 4dB
		3	24dBm	±3dB	11	8dBm	± 4dB
		4	22dBm	±3dB	12	6dBm	± 4dB
		5	20dBm	±3dB	13	4dBm	± 4dB
		6	18dBm	±3dB	14	2dBm	± 5dB
		7	16dBm	±3dB	15	0dBm	± 5dB

2. PERFORMANCE

Item	Description	Specification	
5	Output RF Spectrum (due to modulation)	GSM850/EGSM	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-63
		3,000~ <6,000	-65
		6,000	-71
		DCS/PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-65
		3,000~ <6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	GSM850/EGSM	
		Offset from Carrier (kHz).	Max. dBm
		400	-19
		600	-21
		1,200	-21
		1,800	-24

2. PERFORMANCE

Item	Description	Specification		
6	Output RF Spectrum (due to switching transient)	DCS/PCS		
		Offset from Carrier (kHz).		Max. dBm
		400		-22
		600		-24
		1,200		-24
		1,800		-27
7	Spurious Emissions	Conduction, Emission Status		
8	Bit Error Ratio	GSM850, EGSM BER (Class II) < 2.439% @-102 dBm DCS, PCS BER (Class II) < 2.439% @-102 dBm		
9	RX Level Report Accuracy	±3 dB		
10	SLR	14±3 dB		
11	Sending Response	Frequency (Hz)	Max.(dB)	Min.(dB)
		100	-12	-
		200	0	-
		300	0	-12
		1,000	0	-6
		2,000	4	-6
		3,000	4	-6
		3,400	4	-9
		4,000	0	-
12	RLR	4±3 dB		

2. PERFORMANCE

Item	Description	Specification		
13	Receiving Response	Frequency (Hz)	Max.(dB)	Min.(dB)
		100	-12	-
		200	0	-
		300	2	-7
		500	*	-5
		1,000	0	-5
		3,000	2	-5
		3,400	2	-10
		4,000	2	
		* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.		
14	STMR	Over 17 dB		
15	Stability Margin	> 6 dB		
16	Distortion	dB to ARL (dB)	Level Ratio (dB)	
		-35	17.5	
		-30	22.5	
		-20	30.7	
		-10	33.3	
		0	33.7	
		7	31.7	
		10	25.5	
17	Side Tone Distortion	Three stage distortion < 10%		
18	System frequency (26 MHz) tolerance	≤ 2.5 ppm		
19	32.768KHz tolerance	≤ 30 ppm		
20	Ringer Volume	At least 58 dB SPL under below conditions: 1. Ringer set as ringer. 2. Test distance set as 100 cm		

2. PERFORMANCE

Item	Description	Specification			
21	Charge Current	Fast Charge : Typ. 400 mA Slow Charge : Typ. 400mA Total Charging Time : < 3 hours			
22	Antenna Display	Bar Number	Power		
		7	-92 Over		
		7 -> 5	-93 \pm 2		
		5 -> 4	-98 \pm 2		
		4 -> 2	-101 \pm 2		
		2 -> 1	-104 \pm 2		
		1 -> 0	-106 \pm 2		
		0 -> OFF	-106 Under		
23	Battery Indicator	13 level(Full)	100~93%	6	46~39%
		12	92~85%	5	38~31%
		11	84~77%	4	30~24%
		10	76~70%	3	23~16%
		9	69~62%	2 / 2	15~11% / 10~8%
		8	61~54%	1	7~1%
		7	53~47%	0	0%
24	Low Voltage Warning (Blinking Bar)	It alarms 3 times (standby)10% : 1 st warning 5% : 2 nd warning 0% : 3 rd warning It alarms every 1min under 10%(call)			
25	Forced shut down Voltage	3.35 \pm 0.05V			
26	Sustain RTC without battery	Over 30 sec			
27	Battery Type	Lithium-Ion Battery Standard Voltage = 3.7 V Battery full charge voltage = 4.2 V Capacity: 900mAh			
28	Travel Charger	Switching-mode charger Input: 100 ~ 240V, 50/60 Hz Output: 5.1V, 400 mA			

3. TECHNICAL BRIEF

3.1 LG-A258 Functional Block Diagram

The functional component arrangement is mentioned below diagram.

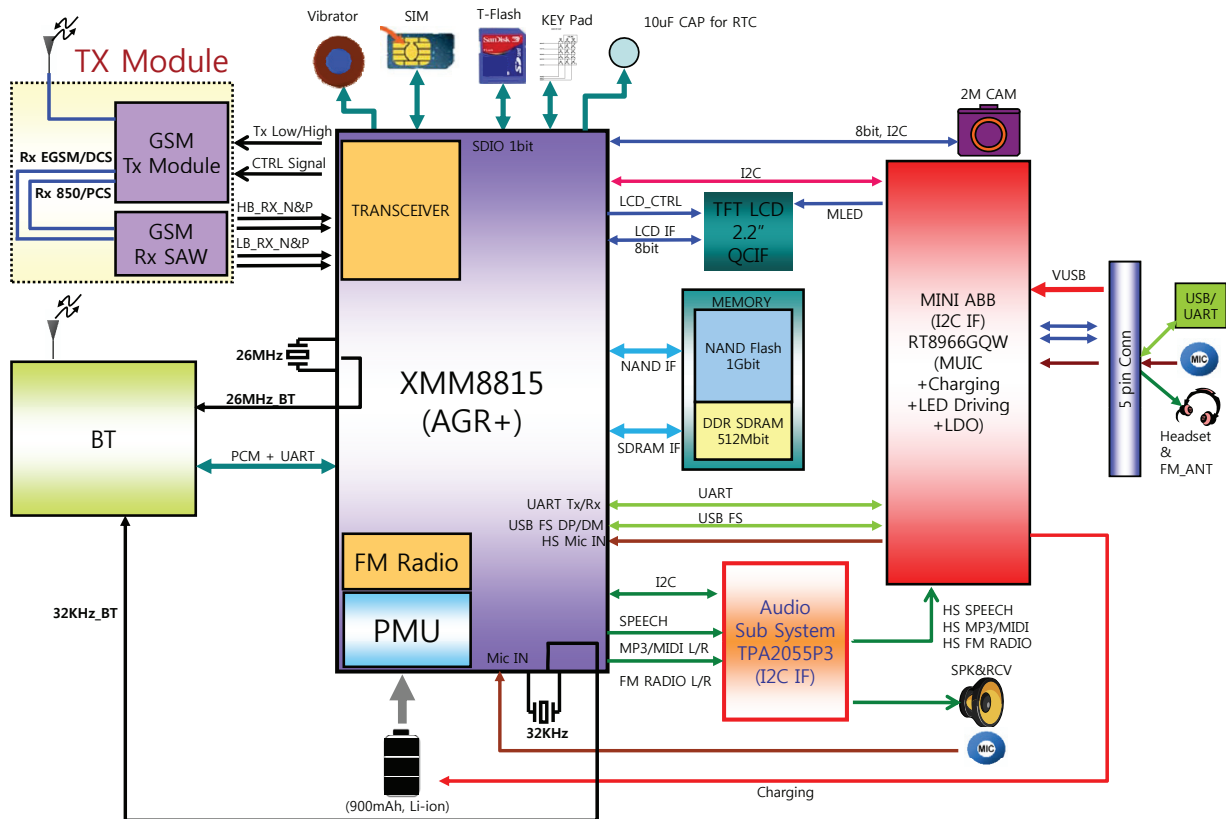


Figure. 3.1.1 LG-A258 Functional Block Diagram

3.2 Digital Main Processor (PMB8815, U101)

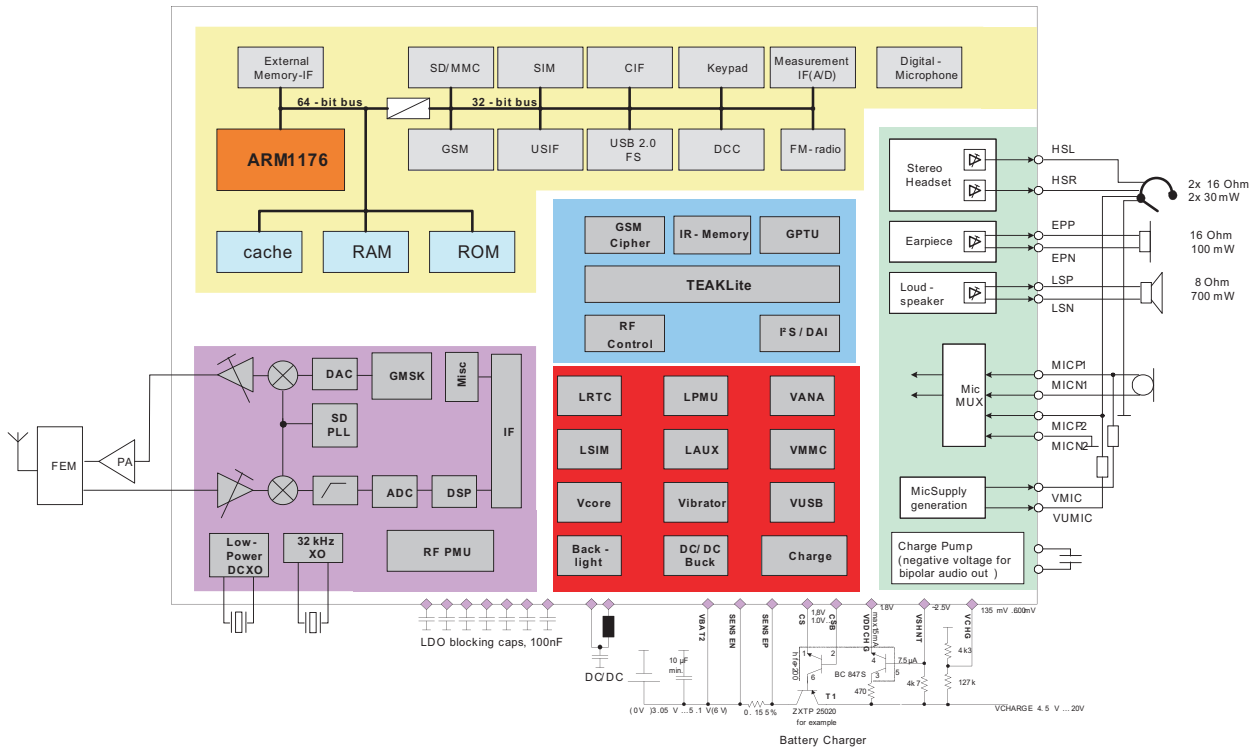


Figure. 3.2.1 X-Gold 215 Hardware Block Diagram

3.2.1 General

Technology:

- SoC, Monolithic, 65 nm CMOS

• Package:

- eWLB, 8x9x0.8 mm

- 0.5 mm pitch

- 240 balls / 6-layer PCB

3.2.2 RF Transceiver

- Dual-band direct conversion receiver
- Tri/Quad-band possible with external circuitry
- Fully integrated digital controlled X0
- Additional buffer for 2 external system clocks
- Fully digital RF-Synthesizer incl. $\Sigma\Delta$ -Transmitter

3.2.3 Baseband

- DSP:
 - 178 MHz TeakLite™
- MCU:
 - ARM® 1176 @ 208 MHz
- MCU RAM:
 - 3.00Mbit
- Memory I/F:
 - 1Gbit NOR flash/One NAND flash/SDR SDRAM
 - 4Gbit NAND flash/DDR SDRAM
- Modem:
 - GPRS class 12, (RX/TX CS1-CS4)
 - EGPRS class 12, (RX MCS1-MCS9, TX MCS1-MCS4)
- Cipher Units:
 - A51/2/3
 - GEA-1/2/3
- Security:
 - OMTP TR0
 - Secure Boot
 - RSA(ROM)/SHA-1(HW accel.)
 - OCDS disabling
 - Certificate Management

- Speech Codec:
 - FR / HR / EFR / NB-AMR
- Audio Codec (running on ARM1176):
 - SP-MIDI
 - SB-ADPCM
 - MP3
 - WB-AMR
 - AAC/AAC+/eAAC+
- Others:
 - DARP (SAIC)
 - TTY
- Customization:
 - E-Fuses

3.2.4 External Memory

- External Bus Unit
 - 16-bit address bus
 - 16-bit address/data muxed bus
 - 1.8V support
- Flash / RAM
 - NOR Type
 - NAND Type(1bit ECC supported)
 - Parallel Flash/Cellular RAM(Page & Burst Mode)
 - 16-bit AD-multiplexed(concurrent usage of DDR interface and AD-multiplexed interface is not supported)
 - 16-bit AAD-multiplexed
 - iNAND Type e.g. oneNAND
 - SDRAM
 - DDR SDRAM : up to 4 Gbit
 - SDR SDRAM : up to 1 Gbit
- Memory card
 - SD/MMC card interface with 1 or 4 data lines

3.2.5 Connectivity

- Up to 3xUSIF (configurable either as SPI or UART), I2C, I2S; Interfaces @ 1.8V
- Direct (U)SIM 1.8/3V
- USB2.0 up to 480 Mbit/s (High Speed) w/ external USB Phy over ULPI interface
- Stereo Headset (Amplifier integrated)
- 3 external analog measurement PIN's
- Bluetooth, A-GPS, WLAN support (I2C, I2S, SPI)

3.2.6 Mixed Signal

- Improved audio performance
- Loudspeaker Audio Class D Amplifier, 700 mW@8 Ω mono for hands-free and ringing
- Stereo Headset 2x30 mW@16 Ω w/o coupling C
- Mono Earpiece 100 mW@16 Ω
- Digital microphone supported
- Differential microphone input

3.2.7 FM Radio

- Integrated FM radio
 - FM Stereo RDS Receiver
 - Sensitivity 2 μ V EMF
 - Support for US & EU bands
 - Stereo recording

3.2.8 Power Management

- Direct-to-Battery Connection
 - LDOs (incl. capless)
 - DC/DC step-down converter
 - DC/DC step-up for white LED supply
- Battery Type
 - Li-Ion
- Charging control
 - Battery temperature
 - Watchdog protection
 - Start-up on flat battery
- External Charger
 - Switch mode
- USB battery charging
 - USB charging spec 1.0 compliant
- Backlight
 - Up to 4 serial white LEDs (integrated LDO)

3.2.9 Display

- Type
 - 128x160, 65k color (serial)
 - QVGA, 262k color (parallel)
- Interface
 - Parallel 8/9bit MIPI-DBI Type B
 - Serial MIPI-DBI Type C
 - Interf. voltage at 1.8V or 2.8V
- gRacR - Display Controller (Hardware)
 - 30 fps Display update without DMA (up to 60 fps) (full or partial)
 - Video post processing Scaling, Rotation (90° steps), Mirroring
 - Overlay with alpha blending
 - Color conversion YUV -> RGB
 - 2D vector graphics (Lines, filled rectangles, Bit block transfer (e.g. sprites, scrolling, antialiased bitmap fonts))

3.2.10 Camera

- 2 Mpx YUV parallel interface
- HW JPEG encoder (39 Mpx/sec)
- 39 MHz Pixel Rate
- 15 fps@ 2 Mpx full resolution

3.2.11 Video Capabilities

- Video Decoding MPEG-4/H.263
 - QCIF@30 fps
 - QVGA@15fps
- Video Encoding MPEG-4/H.263
 - QCIF@15 fps

3.2.12 Audio Capabilities

- Polyphonic ring tones
 - 64 voices MIDI, SP-MIDI
 - FM synthesizer
- AMR-WB
- True ring tones (MP3)
- MP3, eAAC+
- G.722 SB-ADPCM encoding/decoding

3.3 Power Management

A mobile platform requires power supplies for different functions. These power supplies are generated in the integrated power management Unit (PMU). The PMU is designed to deliver the power for a typical standard phone.

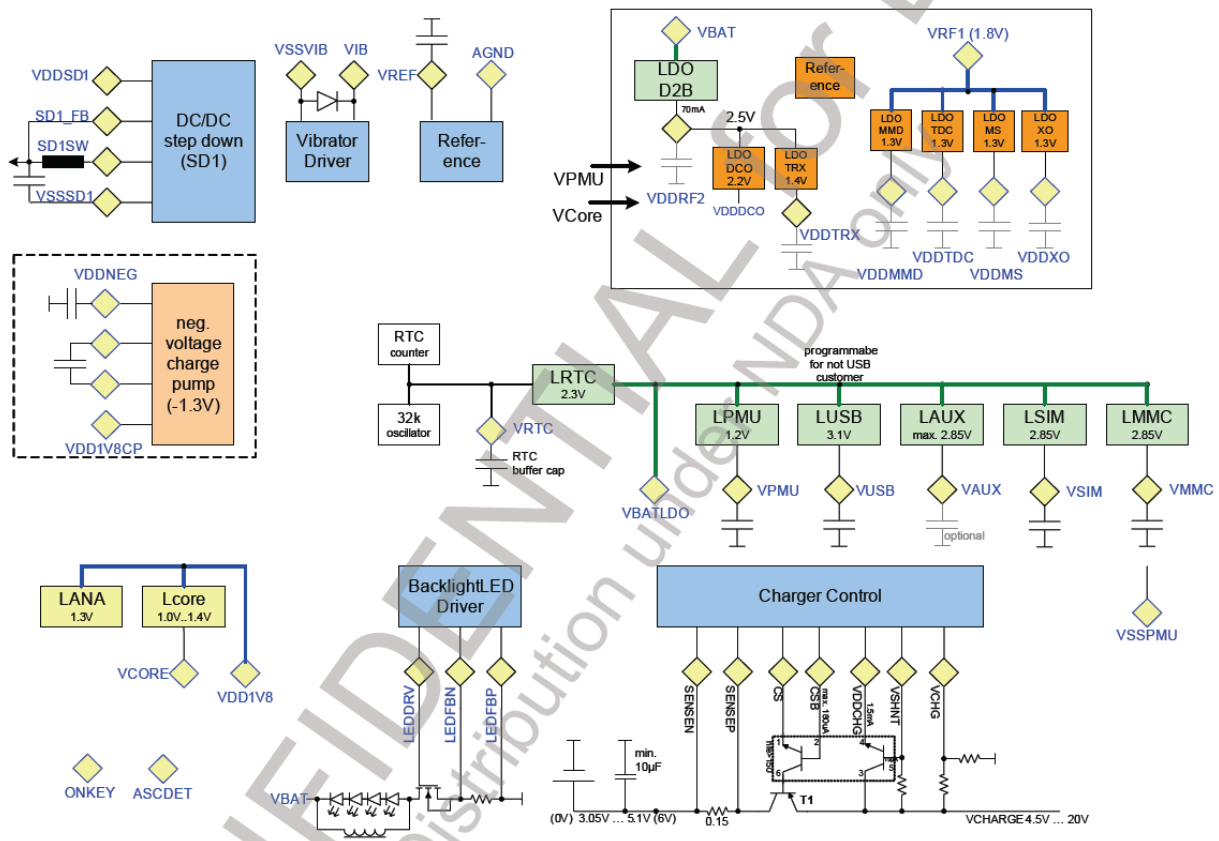


Figure. 3-2-1 Block Figure of the PMU Modules X-Gold tm 215

▪ DC/DC Step Down Converter for 1.8V (SD1)

The DC/DC converter generates a 1.8V supply rail. This voltage rail is used to supply main parts of the system, like the digital core of the chip (via LDO Lcore), some parts of the mixed signal macro, parts of the RF macro and the external memory if a 1.8V memory is used. The efficiency of the DC/DC converter is optimized for an average load current of 100mA. That is the load current estimated for the GSM talk mode.

▪ **Linear voltage Regulators (low dropout) LDOs**

The LDOs are used to generate the supply for the different supply domains not directly supplied out of the DC/DC converter.

▪ **LCORE**

The LCORE LDO provides the VCORE supply used for most of the digital parts of the chip

▪ **LPMU**

The LPMU provides VPMU supply for the PMU supply, e.g. for the startup state machine and analog parts like ADC, sense amplifier etc.

▪ **LUSB**

The LUSB LDO generates the supply for the USB transceiver (output driver and input). If no USB interface is required, LUSB can be used as general purpose LDO.

▪ **LAUX**

The LAUX generates VAUX. It is a general purpose LDO and can be used for different functions depending on the phone application, e.g. for the display or Camera.

▪ **LMMC**

The LMMC generates VMMC. It is a general purpose LDO and can be used e.g. for memory cards

▪ **LSIM**

The LSIM LDO generates the VSIM supply for the SIM card and interface. It is designed to supply Standard SIM cards according ETSI TS 102 221.

▪ **Other LDOs**

- The RF module has implemented several LDO's for different RF power domains.
- The mixed signal module has some LDO's for the audio driver and microphone supply
- The FM receiver has an internal LDO for sensitive RF circuits.

Supply Domain LDO Name	Voltage	Max. Current	Output Cap	Input Domain	Comment
VBAT	0 ... 6.0 V				Operating range is 3.05 V ... 5.5 V, system emergency switch off voltage is about 2.8 V
VDD1V8	1.8 V	450 mA	22 μ F	VBAT	This voltage is generated by the DC/DC converter with 3.3 μ H inductor, The voltage is used for: Memory supply, and via LDO's for digital core supply, mixed signal supply and RF supply.
LCORE	1.2 V	300 mA	2x100 nF	VDD1V8	
LANA	1.3 V	10 mA	No	VDD1V8	No ball
LRTC	2.3 V	2 mA	≥ 100 nF	VBAT	This supply is only used for the HPBG, the 32.768 kHz oscillator and the real-time clock counter required during the sleep- and low-power mode.
LPMU	1.2 V	15 mA	100 nF	VBAT	Supply for the digital part of the PMU including digital control of DC/DC converter. This voltage is also used for the N-DEMOS driver of DC/DC converter and the class-D amplifier and the core PLL.
LUSB	3.1 V	40 mA	100 nF	VBAT	Used for the USB driver supply or as general purpose LDO with programmable output voltages (2.5 V, 2.85 V, 3.1 V)
LAUX	1.5 V ... 2.85 V	150 mA	470 nF	VBAT	General purpose LDO for e.g. Display, Bluetooth, Camera etc. Programmable output voltages are (1.5 V, 1.8 V, 2.5 V, 2.85 V)
LSIM	1.8 V / 2.85 V	30 mA	≥ 100 nF	VBAT	LDO dedicated to the SIM-Card supply. It is chip internal connected to the SIM interface driver.
LMMC	1.5 V ... 2.85 V	150 mA	≥ 470 nF	VBAT	General purpose LDO, targeted for MMC/SD card supply.
VDDNEG	-1.3 V	100 mA	100 nF	VDD1V8	Negative voltage for the bipolar headset audio driver. Generated by a charge pump.

Table. 3.3.1 Power supply Domains (without RF)

3.3.1 Power on and startup

▪ Analog startup Circuit

Because the POR circuit and the LPBG are directly connected to the battery, it is not possible to switch them off. If the battery voltage exceed the power on reset threshold (2.5V), the power on reset is released, the LPMU regulator and the LRTC voltage regulator are switched on. The LPMU regulator starts in its ultra-low power mode

The LPMU regulator generates a control signal (lpmu_OK) that enables the 50KHZ PMU oscillator. The output clock of the oscillator is checked with a fully coded counter. A counter overflow releases the reset (vpmu_rst_n) signal for the small PMU state-machine.

▪ Small first digital State-Machine

The small PMU state-machine is always connected to VPMU After starting from reset the small startup state machine enters the SYSTEM OFF state and only continuous the startup procedure if a switch on event like first connect, on-key, wake up or charge detect occurs.

▪ PMU-main State-Machine

The main PMU state-machine is always connected to VPMU also. The power up sequence driven by the PMU state-machine can be seen in Figure18. After enabling the reference (HPGB) and waiting for the settling time, the battery voltage is measured and compared with the power on threshold. If the battery voltage is high enough, the SD1 DC/DC converter and the LCORE LDO are started. A timer ensures that the supply voltage will be stable before the DCXO is enabled. The DCXO settling time is ensured using a fixed timer. After an overflow of this timer, the reset is released for the rest of the system. The PMU state machine remains in this System-ON state until the system is switched into the OFF state. For example the system sleep mode is completely configured by software(for example switching off the LDO's, switching of the DCXO etc.) and controlled by the VCXO_enable signal. The reason for the startup is stored in the ResetSourceRead register.

▪ Battery Measurement

The ADC and the oscillator for the ADC needs the VDD_ADC supply voltage from the LADC LDO. LADC uses either the charger voltage VDD_CHARGE or VDDRTC as input voltage. The input voltage is selected automatically by a bulk switch circuit. LADC, the ADC and the oscillator are enabled on request for every battery measurement if the charger unit is not running. This is handled by an ADC control block in one of the state-machines. If the charger unit is running the ADC is controlled by the charger state-machine

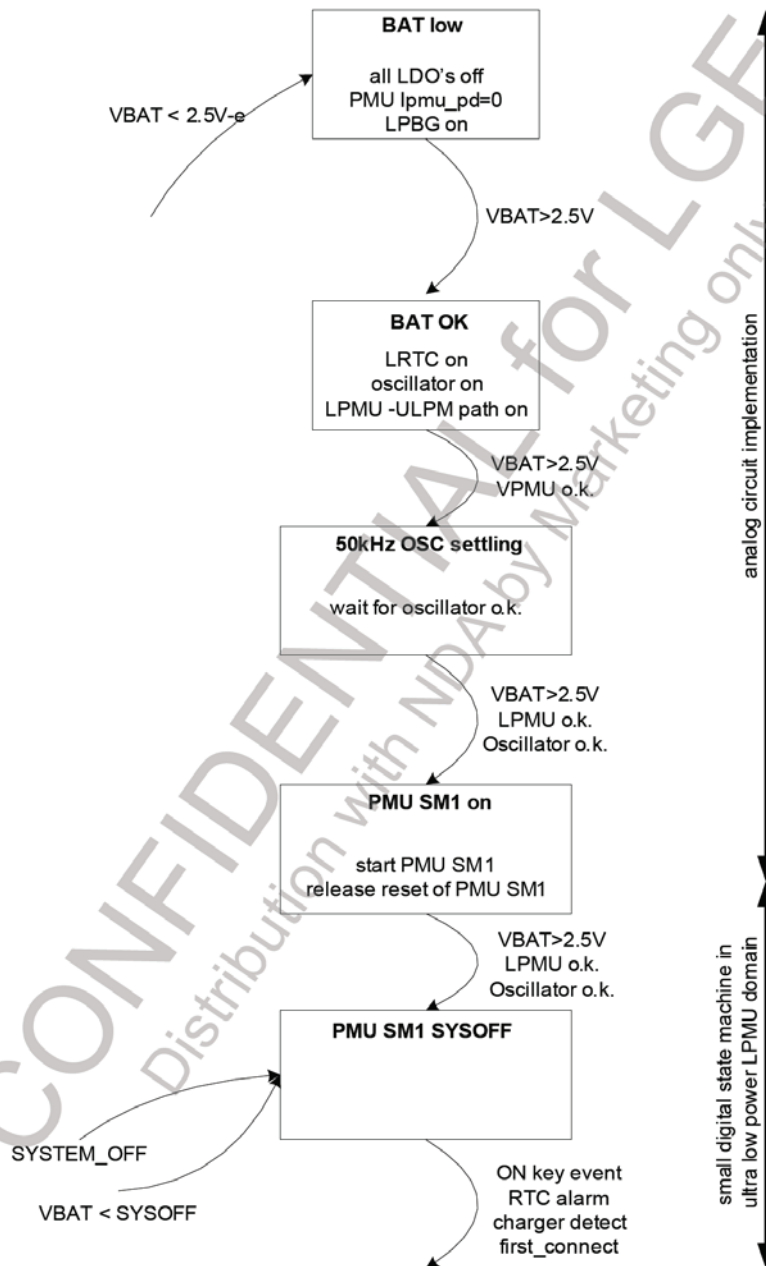


Figure.3.3.2 First Part of the State Machine, Running in Different Power Domains than the Second Part

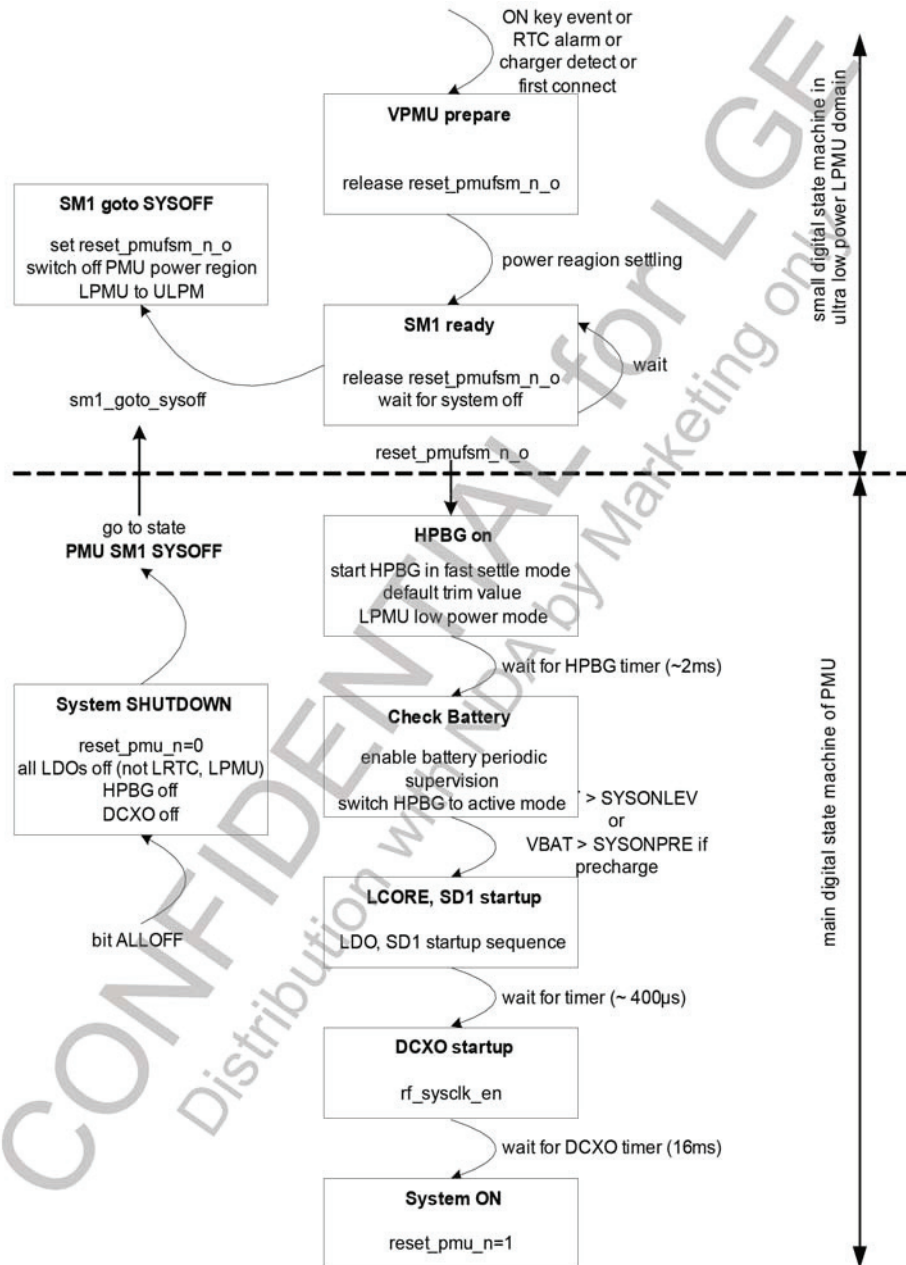


Figure 3.3.3 Second (Main) Part of the Startup State Machine in the VPMU Domain

3.3.2 Switching on due to first connect

If the battery voltage is connected the first time, that means the system enters the first time the SYSOFF state, this is stored in a first connect flag. If the first connect flag is set, the system will start immediately and not wait for any other system on event in the SYSOFF state.

3.3.3 Switching on due to on-Key event

The on key is connected to the ONKEY pad. The ESD protection and the input structure of this pad are connected to VRTC. If the ONKEY pad is forced to VRTC by an external key or similar circuit, the system starts. The ONKEY is sampled with the PMU clock. It has to be sampled four times high before a valid on event is generated. The status of the ON key can be read in the PMU registers, so it can be used as a functional key during phone operation also

3.3.4 Switching on due to RTC alarm

The real time clock can generate a wakeup signal called RTC alarm. This signal is sampled from the state-machine and after successfully detecting a high, the system is switched on.

3.3.5 Switching on due to charging

When a battery with a voltage below the SSONLEV level is inserted, the state machine will not start the system. As long as the battery voltage stays lower than SYSONLEV the system will stay off. The only possibility to start up the system is due to an external charger.

If an external charger is connected and detected and the battery is charged above the SYSONPRE voltage level the system will start up.

The PMU main state machine waits in the Check battery state until the battery voltage condition is fulfilled. The charger state machine provides the necessary pre-charge indication signal. This pre-charge signal is denounced in a small counter to have a stable signal. This is important, especially in half/full-wave charging where the charger detection is switching between charger detected/not detected according the AC supply frequency. reasons

For details on pre-charging see the charger chapter. The charger is controlled by an independent state machine. The pre-charge signal is used to trigger the pre-charge signal is used to trigger the pre-charge functionality. The charger state machine fully control the pre-charge, the PMU-state machine now changes to state HPBG on state and the system starts. This state change is indicated to the charger state-machine to enable the charger watchdog for safety

3.3.6 Power Supply Start-up sequence

In order to avoid an excessive drop on the battery voltage caused by in-rush current during system power-on, possibly leading to system instability and “hick-ups” a staggered turn-on approach for the regulators is implemented. The regulators are turned on in a well defined sequence, thus spreading the in-rush current transients over time.

The IO's of X-GOLD TM 215 are isolated in OFF mode (core supply is off). The isolation signal is controlled by the PMU state machine. This ensures that the PADs are in a well defined state during core supply settling. This allows to power up the LCORE core regulator and wait for the core to reach reset state before powering up the I/O supply regulators.

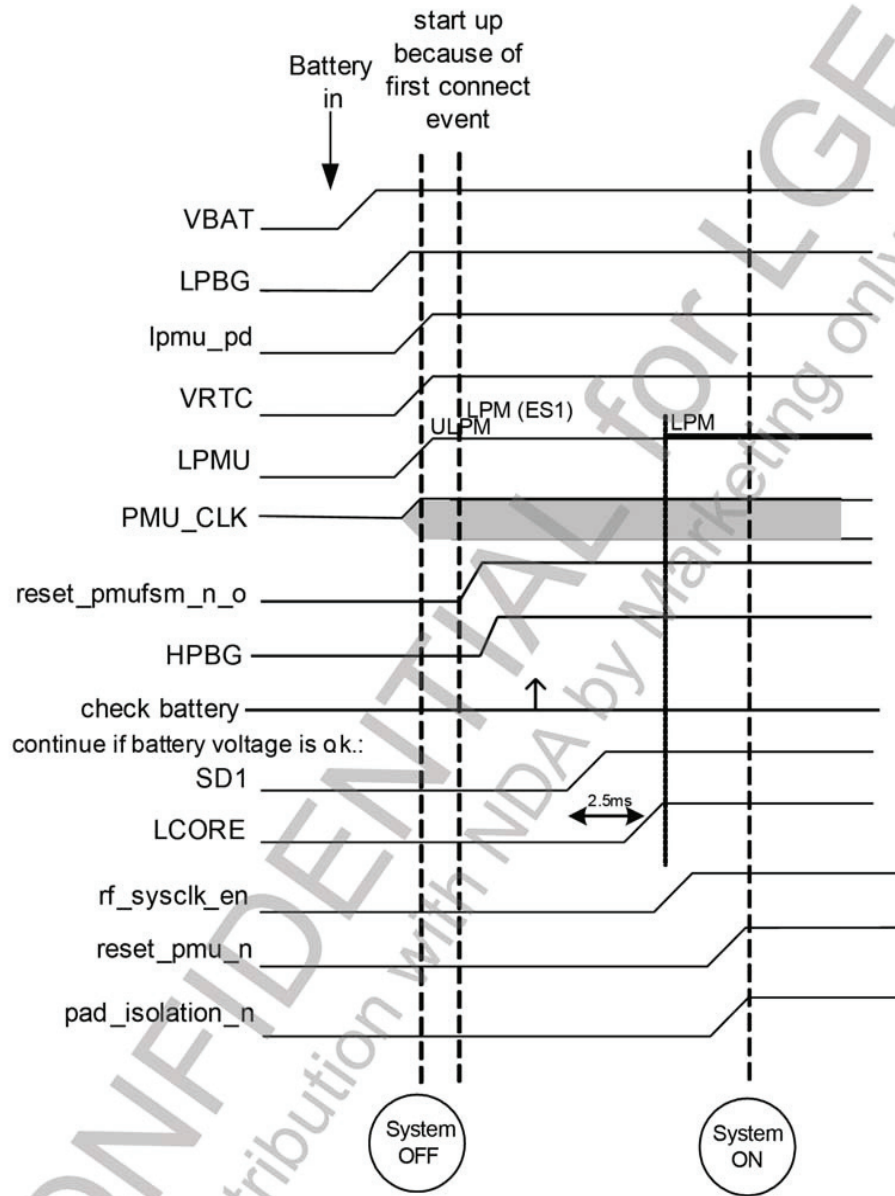


Figure 3.3.4 Start Up Sequence (triggered by First Connect Event)

3.3.7 External Reset Handling

The chip reset can be controlled by an external RESET_N ball. If this ball is pulled low, the chip will be reset. All PMU registers are reset during the external reset including LSIM control bits. The PMU statemachines are also not reset from the external reset. An SW or watchdog reset will not reset the PMU registers. A SW and Watchdog reset is seen on the reset_n pad to allow the reset of external devices. Basically there are three reset sources, first the reset signal controlled by the PMU (reset_pmu_n_o), second the reset signal controlled by the SCU (resetout_o) and third the external reset (RESET_N). The SCU reset is triggered by SW (for example due to a SW reset or watchdog reset). The PMU reset is controlled by the PMU state machine. The output of the reset handling block is the reset_postscu_n_o signal. This signal controls for example the μ C subsystem and releases reset for the controller. During normal start up, the PMU releases the reset_pmu_n_o signal after entering the SYSTEM ON state. At this time the resetout_o signal is high, the RESET_N pad is not pulled low and therefore the reset_postscu_n_o signal follows the reset_pmu_n_o signal. That means the μ C reset will be released and the μ C starts operation. If the SW triggers an external reset via the SCU, signal resetout_o will be forced to low for a certain time and RESET_N will be forced to low by the open drain driver. At the same time the feedback to the SCU will be masked to not reset the baseband. The RESET_N pad is in the VDDRTC domain but the internal pull up is connected to the VDD_VDIG1 (1.8V) domain. That allows the pad to be used as reset for external devices running in the VDD1V8 domain. The RESET_N pad can also be used to monitor the chip internal reset condition during startup.

The open drain driver is a weak driver, that means it can be forced to high during debug from external pushing some current into the pad. In testmode signal reset_pmu_n_o is high, that means the chip reset is fully controlled from external

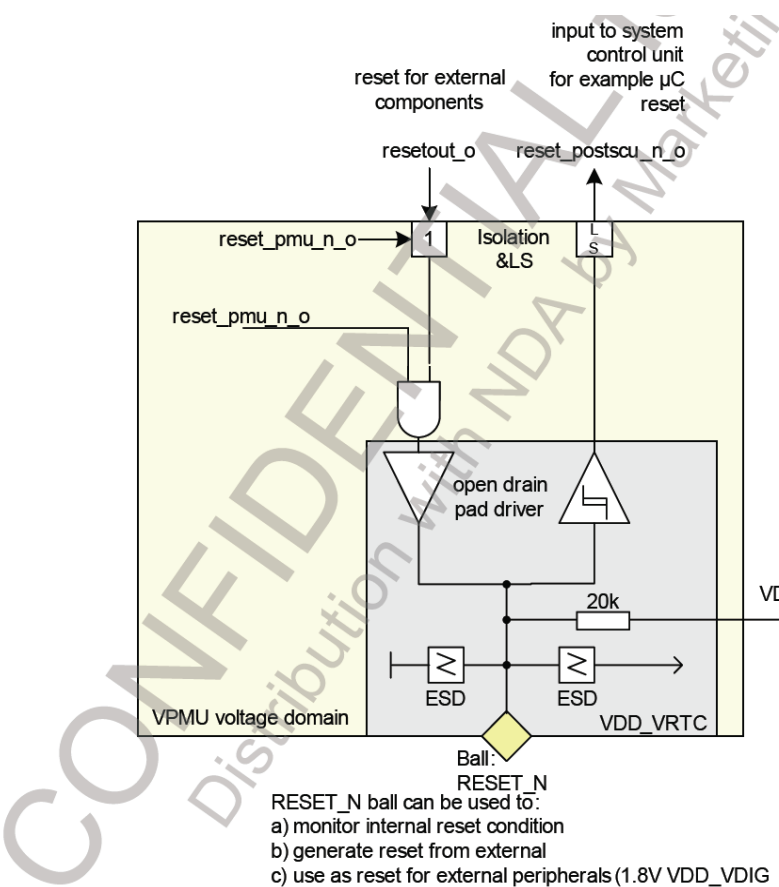


Figure 3.3.5 PMU, CGU and External Reset

3.3.8 Sysclock Switching

The PMU controls the `rf_sysclk_en` signal of the DCXO in the RF macro. During startup the PMU enables the DCXO. After the system is running the DCXO is controlled by the SCU of the baseband by using the `vcxo_enable` signal. This is handled by a dedicated logic in the PMU, see **Figure 3.3.6**. As long as `rf_sysclk_en_pmu`, the output of the PMU state-machine is high, `vcxo_enable` controls the `rf_sysclk_en` signal to the RF. If `rf_sysclk_en_pmu` is low, the DCXO is switched off, independent from `vcxo_enable`.

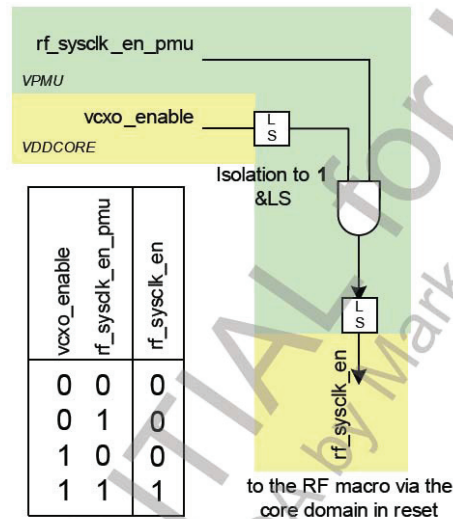


Figure 3.3.6 How sysclock Enable is Routed in the PMU

3.3.9 Undervoltage Shutdown

In active mode the PMU periodically measures the battery voltage using the ADC from the charger unit. If the battery is measured to be below the programmable shut-down level (called SYSOFF), the system changes to OFF mode. This is done via the SHUTDOWN state of the PMU state machine. (see chapter switch OFF)

3.3.10 Software Reset

A software reset does not affect any PMU register. The PMU register are reset with the `reset_pmufsm_n_o` signal. That means all PMU register are reset in OFF state. For details about the SW reset see chapter **External Reset Handling**.

3.3.11 PMU Clock

During the first startup (for example plugging in a battery) a PMU internal oscillator is used for generation of the PMU clock (`pmu_clock`). The frequency is slightly above 32 kHz (typ. 50 kHz) to be out of the audio band also for worst case devices. After first startup the software shall enable the 32 kHz crystal oscillator. It is not possible to use the 32 kHz oscillator during first startup, because the settling time of the oscillator can be quite long. After the 32 kHz oscillator is running and settled the software shall switch the PMU clock to the 32 kHz clock and disable the internal PMU oscillator for power saving reasons. The 32 kHz oscillator shall never be disabled after the PMU clock has been switched. The ADC in the charger unit has it's own oscillator generating a frequency of about 10 MHz. This oscillator is running during charging and during battery measurements triggered by the PMU. It is off otherwise.

3.3.12 System Sleep Mode

The sleep mode is controlled by using the VCXO_enable signal. This signal is used to switch the LDO's and the DC/DC converter SD1 in a programmable way into its low power mode (PFM). In addition DC/DC converter SD1 can be configured to change the output voltage to a lower value for additional power saving.

VCXO_enable is also used to deactivate the HPBG and setting LDO LPMU in the ultra-low-power mode. In addition the DCXO is switched off by the VCXO_enable signal. The VCXO_enable signal is also used to switch some LDO's (software configured) to sleep and/or off mode or to change the output voltages of said LDO's. The state of the main PMU state machine is not changed due to VCXO_enable.

3.3.13 DC/DC Pre-Load Register Handling

The DC/DC converter works in different modes. If the mode is switched from PFM to PWM the pulse-width of the DC/DC converter depends on the current battery voltage (and on the output voltage). The PMU state-machine knows the battery voltage because of the battery supervision function. Depending on this value it selects a startup pulse-width for the DC/DC converter out of a register table. (4-values)

3.3.14 Power Down Sequence

Setting bit OFF in the GeneralControl register switches the system into OFF mode. After the turn off event, the state-machine switches to the SHUTDOWN state. The reset_pmu_n_o signal changes to low, the I/O pads are isolated using the padisolation_n signal, the LCORE LDO and the SD1 DC/DC converter are switched off, the LPMU LDO is switched to ultra-low power mode, the DCXO is turned off and the bandgap buffer is disabled. Before switching OFF the software shall have enabled the 32 kHz oscillator and has switched the PMU clock to the 32 kHz clock to archive the target OFF current

3.4 FEM with integrated Power Amplifier Module (SKY77550, U301)

3.4.1 Internal Block Diagram

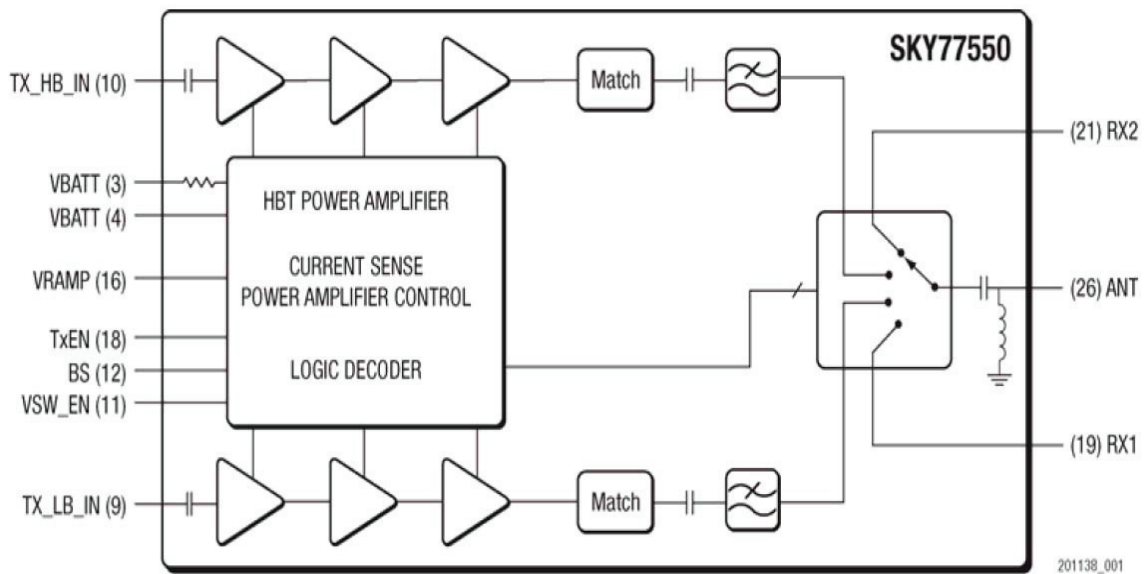


Figure. 3.4.1 SKY77550 FUNCTIONAL BLOCK DIAGRAM

3.4.2 General Description

SKY77550 is a transmit and receive Front-End Module (FEM) with Integrated Power Amplifier Control (iPAC™) for Dual-band cellular handsets comprising GSM850/900 and DCS1800/ PCS1900 operation.

Designed in a low profile, compact form factor, the SKY77550 offers a complete Transmit VCO-to-Antenna and Antenna-to-Receive SAW filter solution. The FEM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation.

The module consists of a GSM850/900 PA block and a DCS1800/PCS1900 PA block, Impedance matching circuitry for 50 ohm input and output impedances, Tx harmonics filtering, high linearity / low insertion loss RF switch, and a Power Amplifier Control (PAC) block with internal current sense resistor. The two Hetero junction Bipolar Transistor (HBT) PA blocks, a BiFET PAC and switch control circuit are fabricated onto a single Gallium Arsenide (GaAs) die. One PA block supports the GSM850/900 bands and the other PA block supports the DCS1800/PCS1900 bands.

Both PA blocks share common power supply pads to distribute current. The output of each PA block and the outputs to the two receive pads are connected to the antenna pad through an RF switch. The GaAs die, Switch die and passive components are mounted on a multi-layer laminate substrate.

The assembly is encapsulated with plastic overmold.

3. TECHNICAL BRIEF

Mode	Input Control Bits		
	VSW_EN	TxEN	BS
STANDBY	0	0	0
Rx1 ¹	1	0	0
Rx2 ¹	1	0	1
Tx_LB	1	1	0
Tx_HB	1	1	1

¹ Rx1 and Rx2 are broadband receive ports and each supports the GSM850, GSM900, DCS, and PCS bands.

Table 3.4.1 Band SW Logic Table

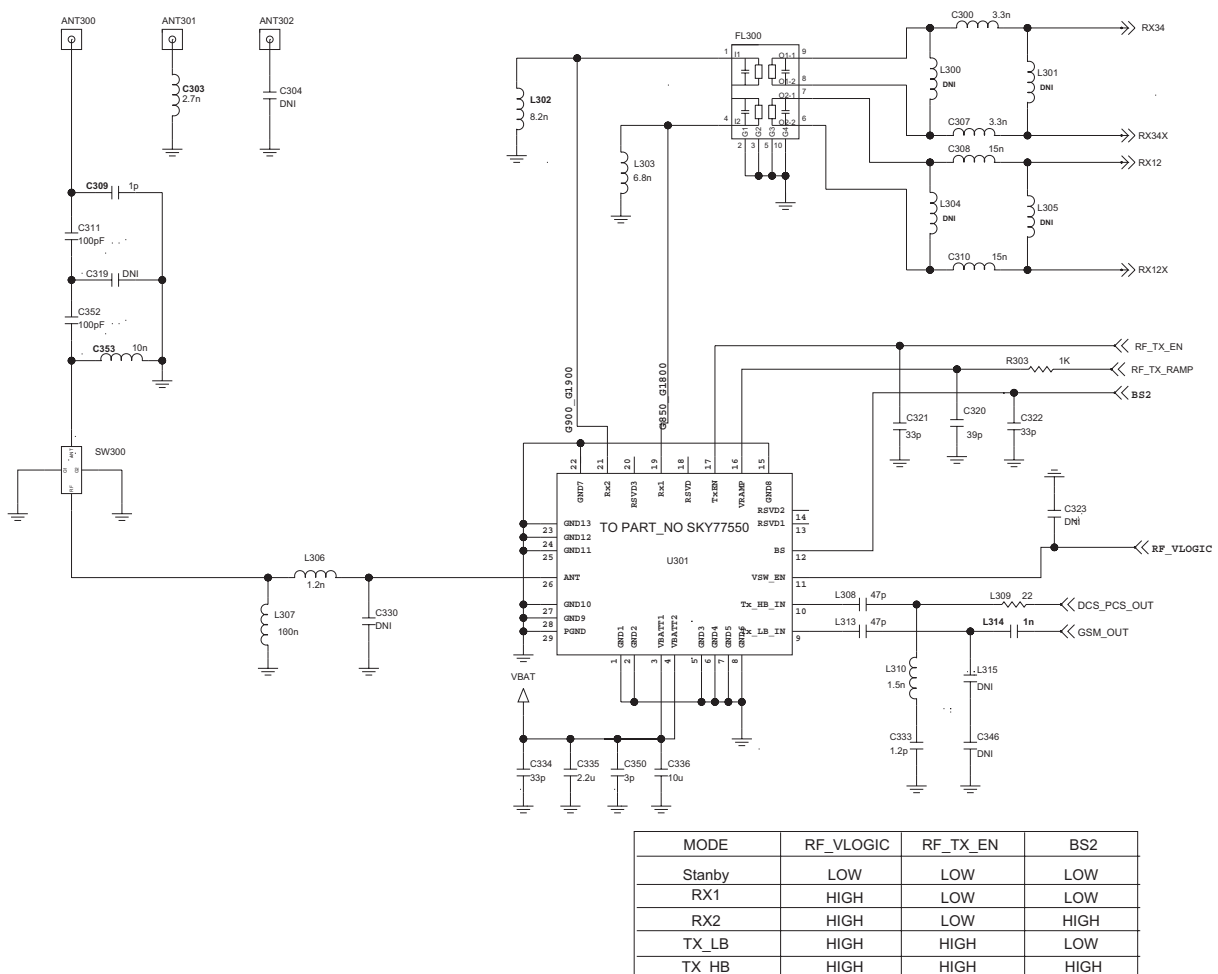


Figure 3.4.2 FEM CIRCUIT DIAGRAM

3.5 Crystal(26 MHz, X100)

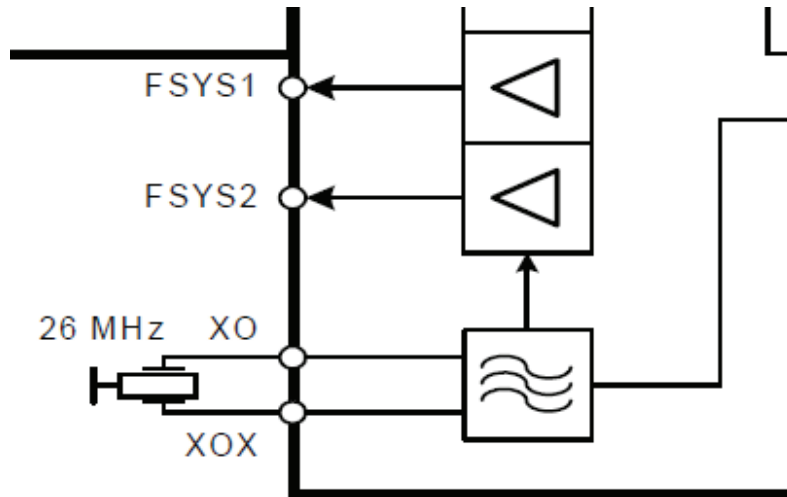


Figure. 3.5.1 Crystal Oscillator External Connection

Reference frequency is generated by a digitally adjustable 26 MHz oscillator, designed for 8 pF crystals. This frequency serves as comparison frequency within the RF-PLL and as clock frequency for the digital circuitry. The reference clock can also be applied to external components like Bluetooth or GPS, via two independently controllable FSYS output pins.

3.6 RF Subsystem of PMB8815 (U101)

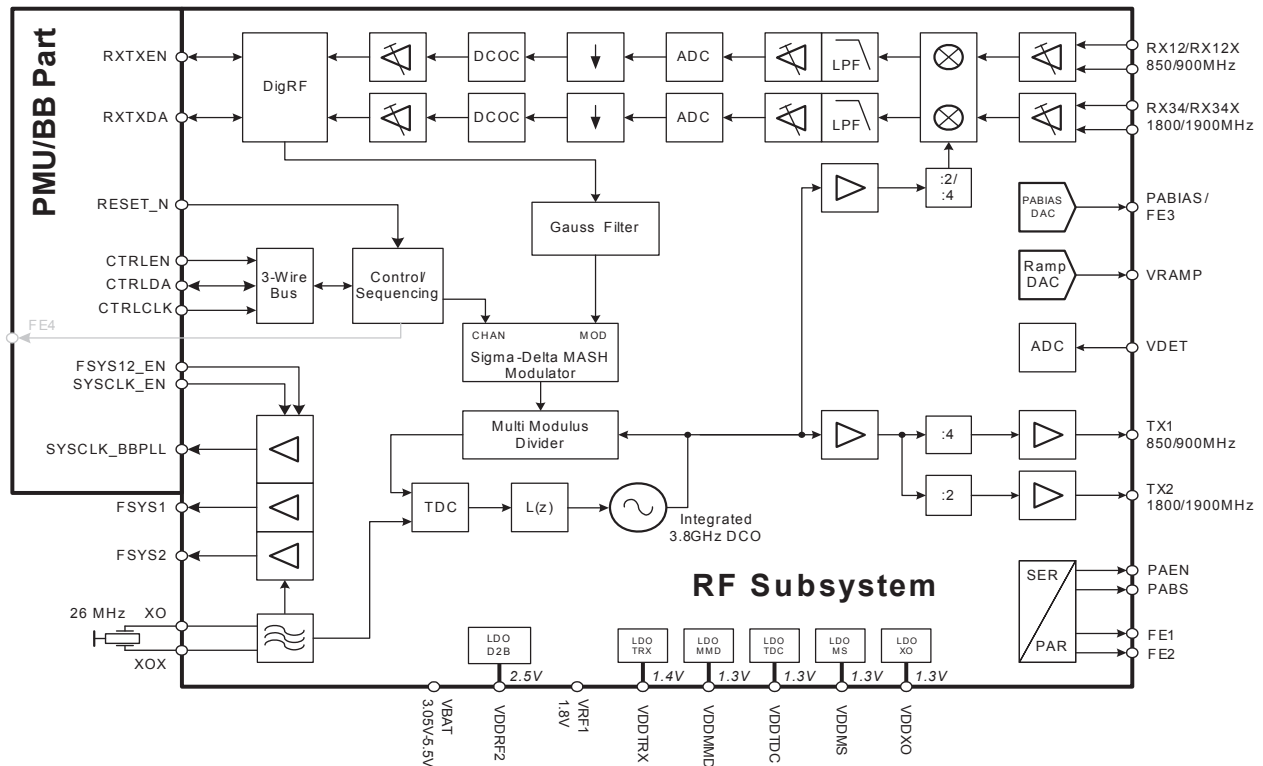


Figure. 3-6-1 Block DIAGRAM of RF Subsystem

3.6.1 GENERAL DESCRIPTION

The X-GOLD™ 215 RF subsystem is designed for dual-band GSM voice and data applications (GPRS class 12). The system can be configured to support one low band, GSM850 or EGSM900, and one high band, DCS1800 or PCS1900. A block diagram of the RF subsystem is given in Figure 3-6-1.

3.6.2 FUNCTIONAL DESCRIPTION

3.6.2.1 Receiver

The X-GOLD™ 215 dual-band receiver is based on a Direct Conversion Receiver (DCR) architecture. Input impedance of the LNAs is optimized to achieve a matching without (external) high quality inductors. By use of frequency dividers (by 2/4) the LO frequency is derived from the RF frequency synthesizer. The receive path is fully differential to suppress the on-chip interferences and reduce DC-offsets. The analog chain of the receiver contains two LNAs (low/high band), a quadrature mixer followed by an analog baseband filter and 14-bit continuous-time delta-sigma analog-to-digital converter. The filtered and digitized signal is fed into the digital signal processing chain, which provides decimation, DC offset removal and programmable gain control.

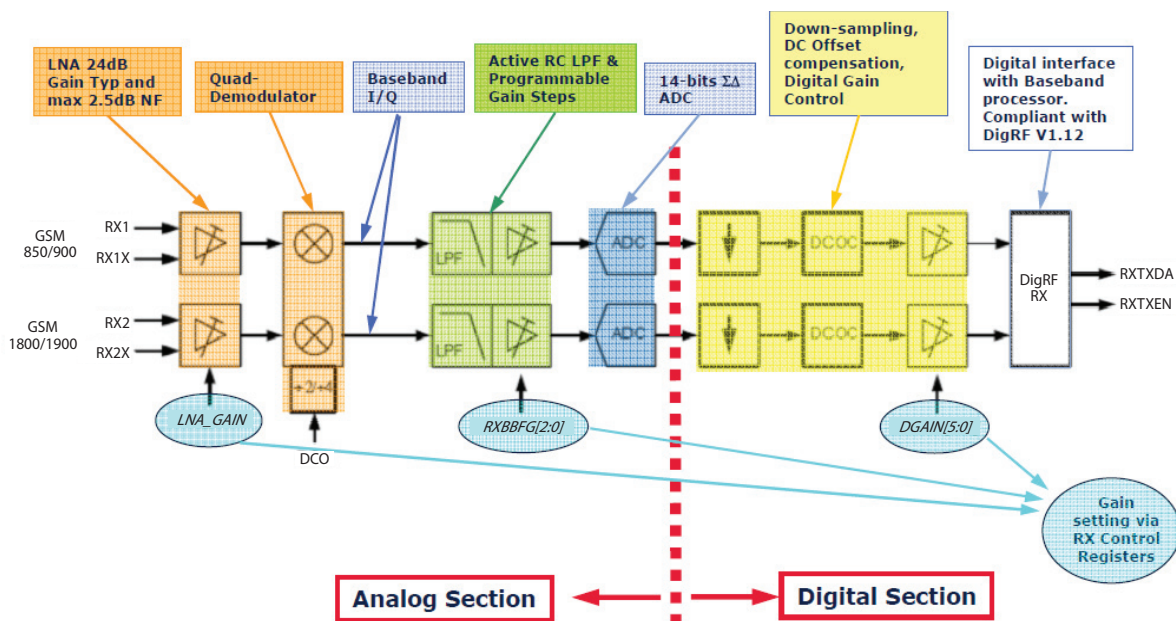


Figure. 3.6.2 RECEIVER CHAIN BLOCK DIAGRAM

3.6.2.2 Transmitter

The GMSK transmitter supports power class 4 for GSM850 or GSM900 as well as power class 1 for DCS1800 or PCS1900. The digital transmitter architecture is based on a fractional-N sigma-delta synthesizer for constant envelope GMSK modulation. This configuration allows a very low power design without any external components. Up- and down-ramping is performed via the ramping DAC connected to VRAMP.

RF synthesizer

The RF subsystem contains a fractional-N sigma-delta synthesizer for the frequency synthesis. Respective to the chosen band of operation the phase locked loop (PLL) operates at twice or forth of the target signal frequency. In receive operation mode the divided output signal of the digital controlled oscillator output (DCO) serves as local oscillator signal for the balanced mixer. For transmit operation the fractional-N sigma-delta synthesizer is used as modulation loop to process the phase/frequency signal. The 26 MHz reference signal of the phase detector incorporated in the PLL is provided by the reference oscillator.

3.6.2.3 Front-end/PA Control Interface

Two outputs (FE1, FE2) for direct control of antenna switch modules enable to select RX- and TX-mode as well as low- and high-band operation. An extra band select signal PABS for the power amplifier is used, to support discrete PA and switching modules. Time accurate power dissipation of the PA is achieved by the control signal PAEN. A minor set of power amplifiers require a bias voltage to enhance power efficiency. Support of this power amplifiers is achieved by the implemented bias DAC.

3.6.2.4 Power Supply

To increase power efficiency less sensitive parts of the RF subsystem are supplied by the DCDC converter situated in the PMU subsystem. Conversion of the 1.8 V output voltage of the DCDC to the 1.3 V circuit supply voltages is achieved by several Low-DropOut regulators (LDO). One embedded direct-to-battery LDO provides the 2.5 V supply voltage for the remaining circuits. This voltage is also used to generate a clean 1.4 V supply voltage via an additional LDO.

LG-A258 is composed of 1 memory. 1Gbit NAND & 512Mbit DDR SDRAM employed on LG-A258.

Figure. 3.7.1 Memory(NAND + DDR SDRAM) Circuit Diagram

3.7.1.1 NAND

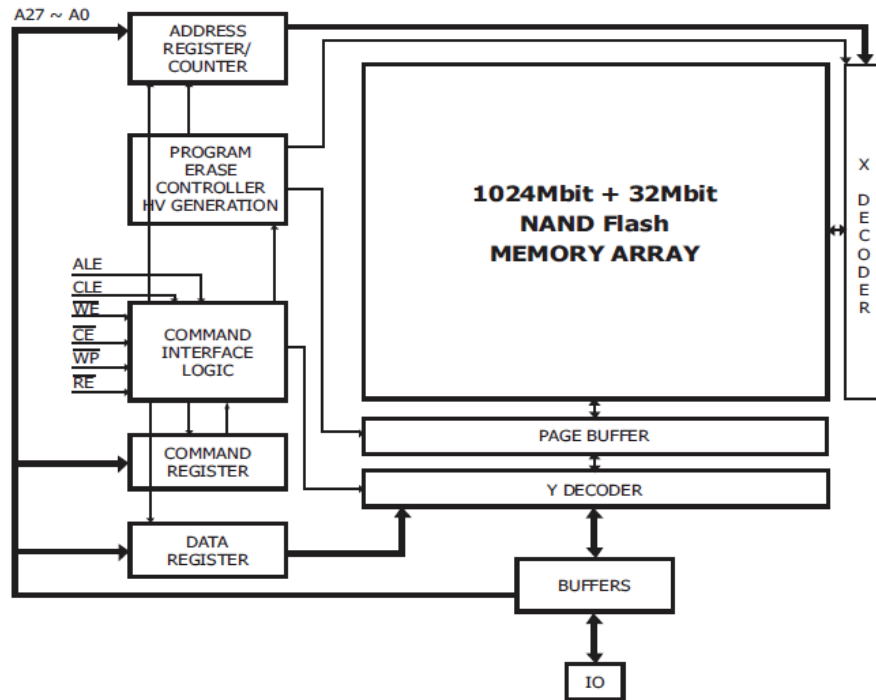


Figure. 3.7.2 NAND Part Block Diagram

[NAND Flash]

- Supply Voltage
 - Vcc = 1.7 - 1.95 V
- Memory Cell Array
 - (1 K + 32) Words x 64 pages x 1024 blocks
- Page Size
 - (1 K + 32 spare) Words
- Block Size
 - (64 K + 2 K spare) Words
- Page Read / Program
 - Random access : 25us (max.)
 - Sequential access : 45ns (min.)
 - Page program time : 200us (typ.)
- COPY BACK PROGRAM MODE
 - Fast page copy without external buffering
- FAST BLOCK ERASE
 - Block erase time: 2.0ms (typ.)
- STATUS REGISTER
- DATA RETENTION
 - 100,000 Program/Erase cycles (with 1bit/528byte ECC)
 - 10 years Data Retention

The device is offered in 1.8 V Vcc Power Supply, and with x16 I/O interface. Its NAND cell provides the most cost effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 1024 blocks, composed by 64 pages. A program operation allows to write the 1056 words page in typical 200 us and an erase operation can be performed in typical 2.0 ms on a 128 K byte block.

Data in the page can be read out at 45 ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.

Commands, Data and Addresses are synchronously introduced using CE, WE, RE ALE and CLE input pin. The on-chip

Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the WP input.

The chip supports CE don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE transitions do not stop the read operation.

The output pin R/B (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/B pins can be connected all together to provide a global status signal.

Even the write-intensive systems can take advantage of the H27S1G6F2B Series extended reliability of 100 K program/erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Data read out after copy back read is allowed.

This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

3.7.1.2 DDR SDRAM

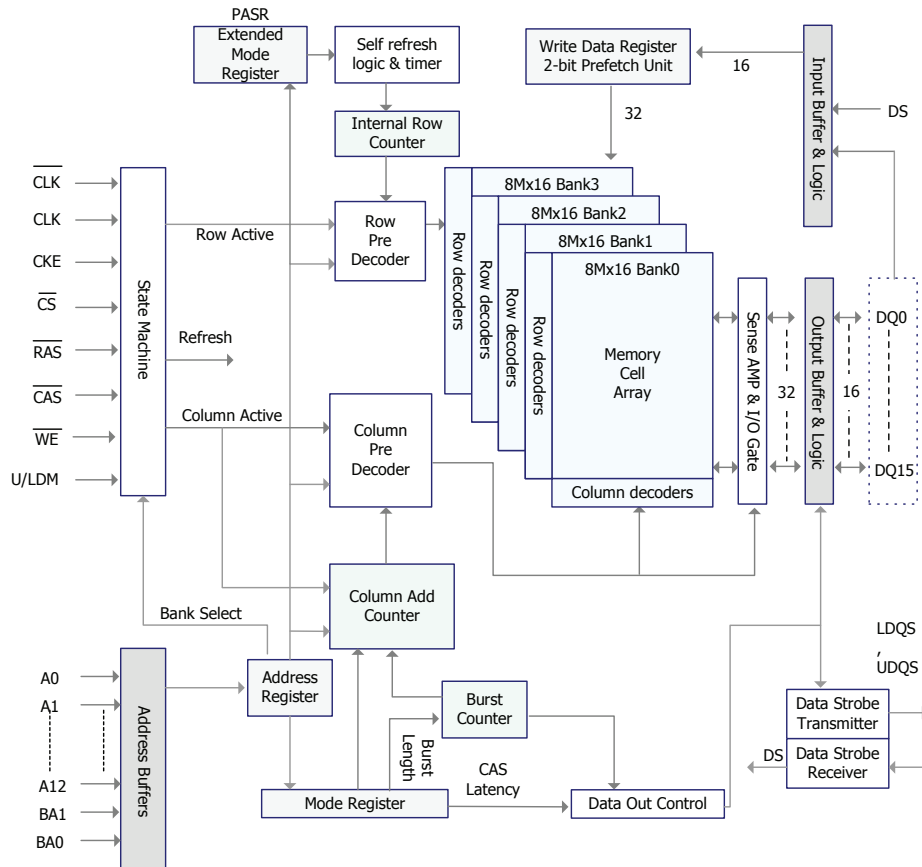


Figure. 3.7.3 DDR SDRAM Part Block Diagram

[DDR SDRAM]

● Double Data Rate architecture
-two data transfer per clock cycle

● x16 bus width

● Supply Voltage
-VDD / VDDQ = 1.7 - 1.95 V

● Memory Cell Array
-8Mb x 4Bank x 16 I/O

● Bidirectional data strobe (DQS)

● Input data mask signal (DQM)

● Input Clock
-Differential Clock Inputs (CK, /CK)

● MRS, EMRS
-JEDEC Standard guaranteed

● CAS Latency
-Programmable CAS latency 2 or 3 supported

● Burst Length
- Programmable burst length 2 / 4 / 8 with both sequential and interleave mode

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{\text{CK}}$	INPUT	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$ (both directions of crossing).
CKE	INPUT	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously.
$\overline{\text{CS}}$	INPUT	Chip Select: $\overline{\text{CS}}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{CS}}$ is considered part of the command code.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	INPUT	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered
BA0, BA1	INPUT	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS, EMRS).
A0 ~ A12	INPUT	Address inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a MODE REGISTER SET command. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. Row Address: A0 ~ A12, Column Address: A0 ~ A9 Auto-precharge flag: A10
DQ0 ~ DQ15	I/O	Data Bus: data input / output pin
LDM ~ UDM	INPUT	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled. HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Data Mask pins include dummy loading internally, to match the DQ and DQS loading. For x16 devices, LDM corresponds to the data on DQ0-DQ7, and UDM corresponds to the data on DQ8-DQ15.
LDQS ~ UDQS	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data. Used to capture write data. For x16 device, LDQS corresponds to the data on DQ0-DQ7, and UDQS corresponds to the data on DQ8-DQ15.
VDD	SUPPLY	Power supply
VSS	SUPPLY	Ground
VDDQ	SUPPLY	I/O Power supply
VSSQ	SUPPLY	I/O Ground
NC	-	No Connect: No internal electrical connection is present.

Table 3.7.1 DDR SDRAM PIN Description Table

3.8 Bluetooth module

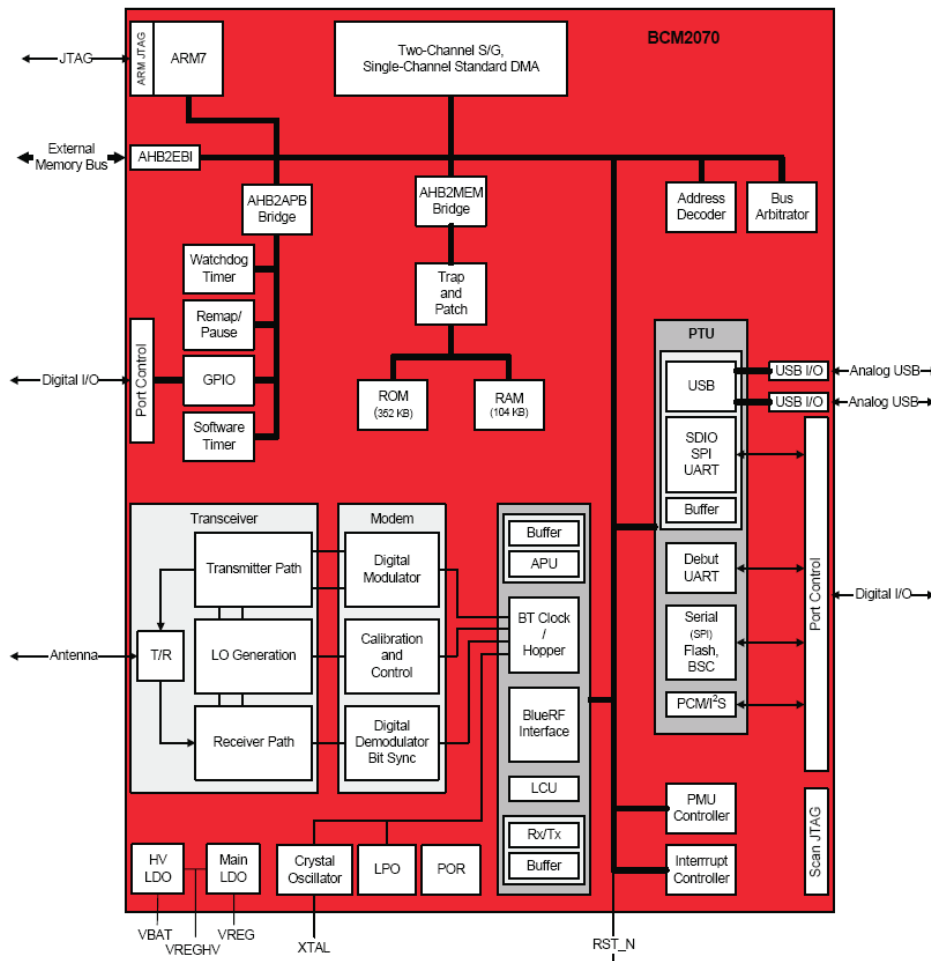


Figure 3.8.1. Bluetooth BLOCK DIAGRAM

This module has an integrated radio transceiver that has been optimized for use in 2.4GHz Bluetooth Wireless systems. It has been designed to provide low-power, robust communications for applications Operating in the globally available 2.4GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and enhanced data rate specification and meets or exceed the requirement to provide the highest communication link quality of service.

3.8.1 Transmitter path

This module features a fully integrated zero IF transmitter. The baseband transmitted data is digitally modulated in the modem block and up-converted the 2.4GHz ISM band in the transmitter path.

The transmitter path consists of signal filtering, I/Q up-conversion, high -output power amplifier(PA), and RF filtering. It also incorporates modulation schemes P/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support enhanced data rate.

• Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK, $\pi/4$ DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

• Power Amplifier

The integrated PA for the BCM2070 is configurable for Class 2 operation, transmitting up to +4 dBm as well as Class 1 operation and transmit power up to +12 dBm at the chip, GFSK, >2.5V supply. Due to the linear nature of the PA, combined with some integrated filtering, no external filters are required for meeting Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications, where Bluetooth is integrated next to the cellular radio, minimal external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions.

Using a highly linearized, temperature compensated design the PA can transmit +12 dBm for basic rate and +10 dBm for enhanced data rates(2 to 3 Mbps). A flexible supply voltage range allows the PA to operate from 1.2V to 3.0V. The minimum supply voltage at VDDTF is 1.8V to achieve +10dBm of transmit power.

3.8.2 Receiver path

The receiver path uses a low IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the device to be used in most applications with no off-chip filtering. For integrated handset operation where the Bluetooth function is integrated close to the cellular transmitter, minimal external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

3.9 SIM Card Interface

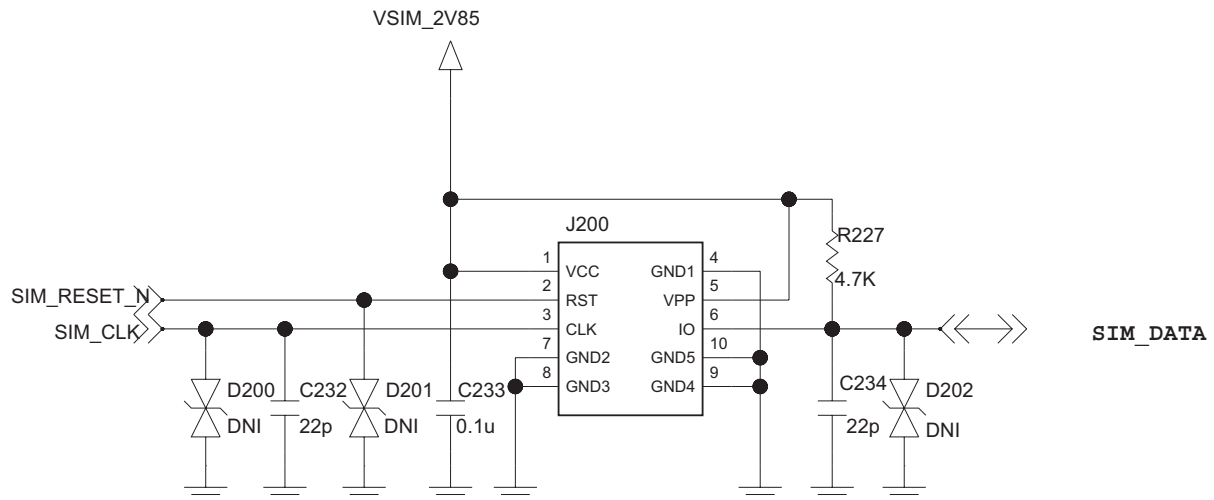


Figure 3.9.1. SIM CARD Interface

The Main Base Band Processor(XMM2130) provides SIM Interface Module.

The XMM2130 checks status Periodically During established call mode whether SIM card is inserted or not, but it doesn't check during deep sleep mode. In order to communicate with SIM card, 3 signals SIM_DATA, SIM_CLK, SIM_RST.

SIM interface scheme is shown in (Figure 3.9.1).

SIM_DATA, SIM_CLK, SIM_RST ports are used to communicate with Main Chip(AGR+NAND)

Signal	Description
SIM_RST_N	This signal makes SIM card to HW default status.
SIM_CLK	SIM card reference clock.
SIM1_DATA	This signal is interface datum.

3.10 LCD Interface

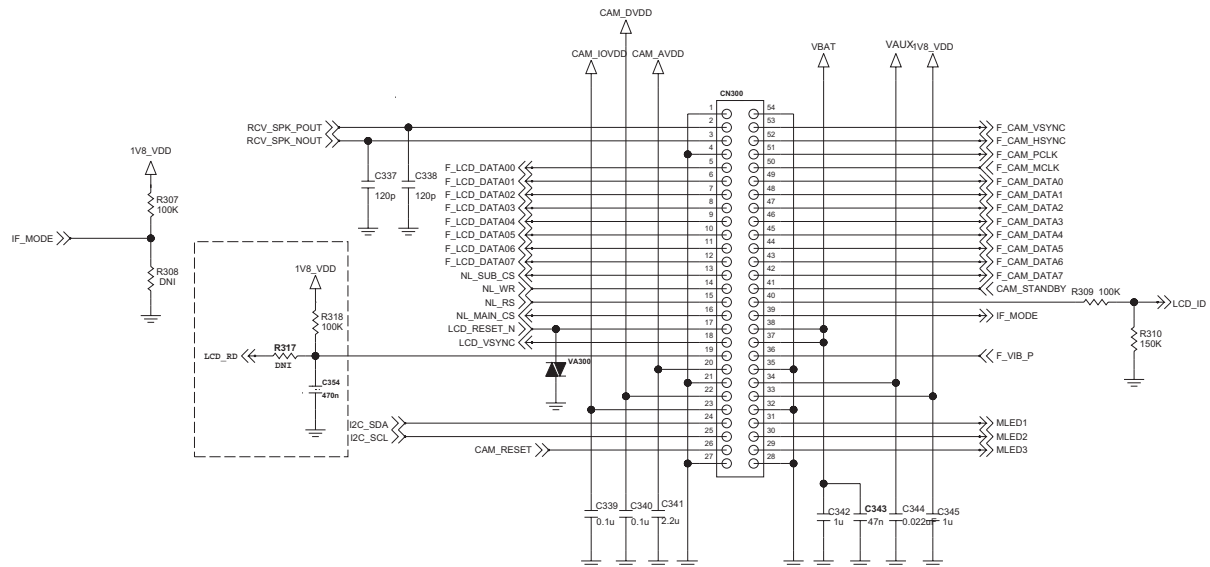


Figure 3.10.1. LCD Interface

The LM220CN1A module is a Color Active Matrix Liquid Crystal Display with an Light Emission diode(LED) Back Light system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally White mode. This TFT-LCD has a 2.2 inch diagonally measured active display area with 176 * RGB * 220 resolution. Each pixel is divided into R,G,B dots which are arranged in vertical stripes. Gray scale or the brightness of the dots color is determined with a 6 bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors.

FEATURES

- Display mode: Transmissive TN mode 262K colors
- LCD Driver IC: ILI9225B (1 chip for Gate & Source Driver)
- Interface : 8bit, 16bit CPU interface
- Backlight: 3 White LED(1 way)
- Standby, Still, Moving mode display
- Low power consumption driving
- Mobile Phone Application

3.11 Vibrator Interface

Support PWM signal which generated by hardware itself via register control direct connect to the VIB and VSSVIB pin from XMM215 without any external component required it is capable to driver the vibrator motor up to 150mA

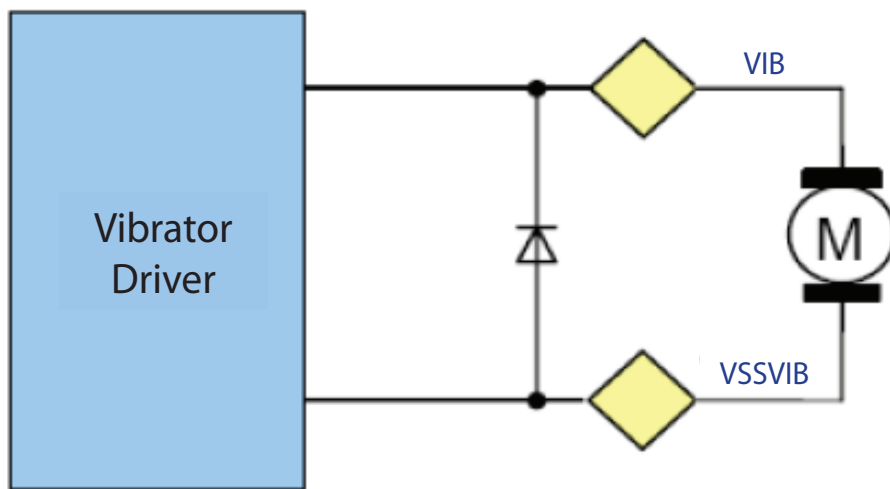


Figure 3.11.1 Vibrator Driver Block Diagram

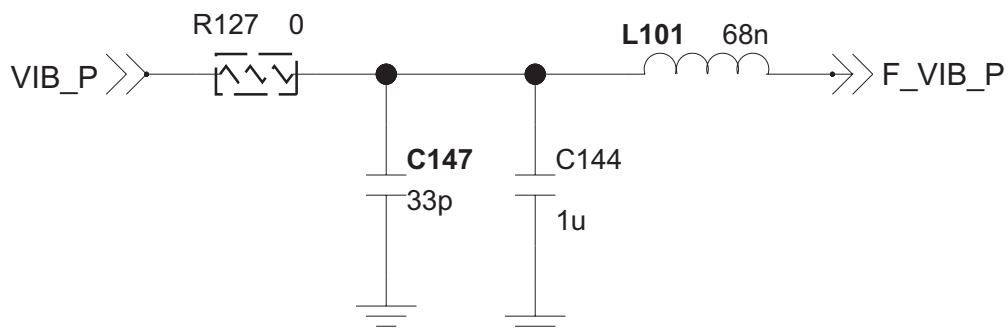


Figure 3.11.2 Vibrator Driver Block

3.12 MINI ABB Interface

The RT8966 is an analog subsystem which includes a linear charger, 4 LDOs, a 4-CH current source, and a multiplexer for USB, UART, microphone, stereo and audio on a single mini/micro USB connector.

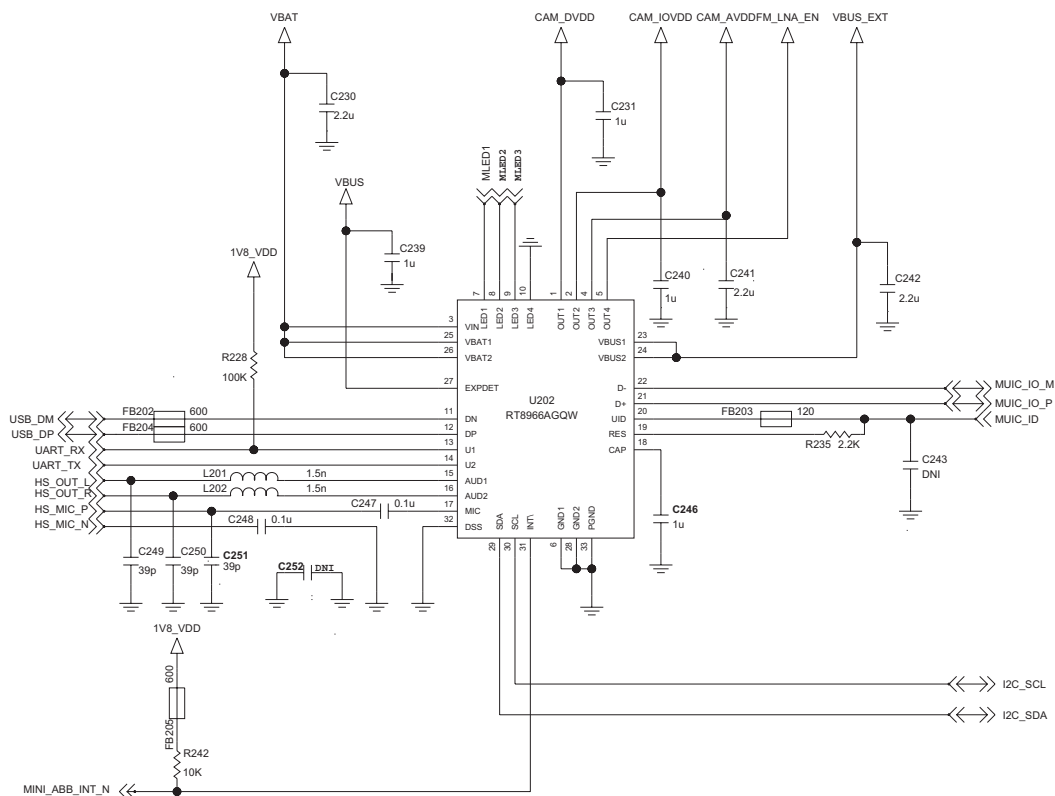


Figure 3.12.1. RT8966GQW CIRCUIT DIAGRAM

3.12.1 Current Source LED Driver for LCD Display

There are four current source LED drivers in the RT8966.

These current sources can be programmed via I2C in the following control registers, Enable and LED Set. These registers include each driver's enable/disable control, source current control, and LED brightness dimming.

The RT8966 provides a constant current for the white LEDs. Each channel supports up to 30mA current and regulates a constant current for uniform intensity. In order to maintain LED constant current, the input voltage must provide the required LED forward voltage and current source dropout voltage. If the forward voltage of the white LEDs is 3.3V, the input voltage should be higher than 3.4V to provide enough voltage headroom for maintaining constant brightness.

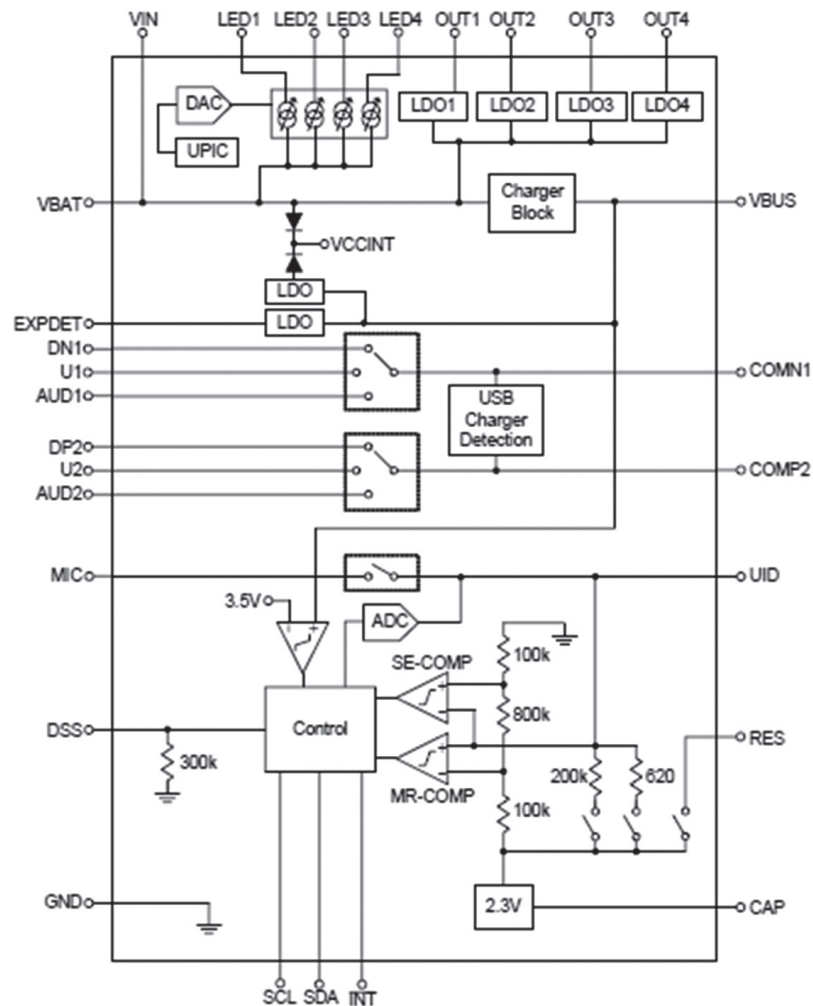


Figure 3.12.2. RT8966GQW FUNCTION BLOCK DIAGRAM

3.12.2 Charging

Charger Description

The RT8966 integrates a single-cell Li-ion battery charger IC with pre-charge mode, a fast charge mode (constant current mode) or constant voltage mode. The charge current is programmable via the I2C interface as shown in the control register address tables, CHG_Ctrl1 and CHG_Ctrl2. The CV mode voltage is fixed at 4.2V. The pre-charge threshold is fixed at 2.6V. If the battery voltage is below the pre-charge threshold, the RT8966 charges the battery with a trickle current until the battery voltage rises above the pre-charge threshold. The RT8966 is capable of being powered up from AC adapter and USB (Universal Serial Bus) port inputs. Moreover, the RT8966 includes a linear regulator (LDO 4.9V, 50mA) for supplying low power external circuitry.

3.12.3 MUIC

(Micro USB Integrated IC - Multiplexing USB, UART and audio on a single micro USB connector)

The USB input provides high speed USB connection. The audio inputs feature negative rail signal operation to realize simple DC coupled headset speakers. The RT8966 provides an internal device detection method by using the USB ID signal pin and the VBUS voltage. The resistor values and VBUS voltage determine the unique detection method of each accessory. The host microprocessor adopts I2C to control the switch position and read the results of the accessory detection. The RT8966 can also detect USB chargers, including dedicated chargers (D+/D-short) and high, power, host/hub chargers.

Switches

The RT8966 provides a multiple input multiplexer to support USB high Speed, UART, stereo audio, mono audio and a microphone. The output of the multiplexer is used to connect to a mini or mtor. When the VBUS voltage is higher than the VB Detect threshold voltage, the RT8966 can turn on and turn off the paths of USB, UART and Audio. However, when the VBUS voltage is lower than the VB Detect threshold voltage, the RT8966 can then only turn on and turn off the paths of stereo audio and mono audio. The following table shows the switch status versus VBUS level.

	USB Switches	UART Switches	Audio Switches
VBUS = High	Allow	Allow	Allow
VBUS = Low	Not Allow	Not Allow	Allow

Table 3.12.1. RT8966GQW SWITCH DETECTION TABLE

3.13 Keypad Interface

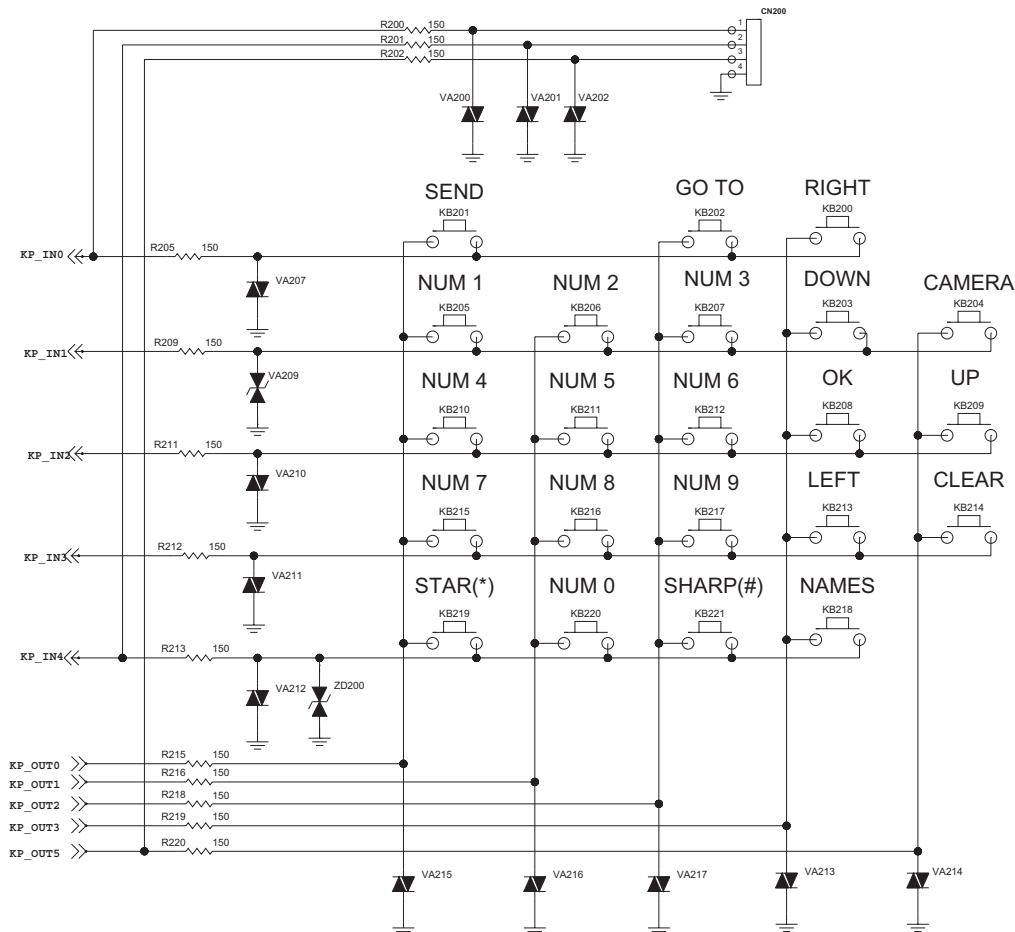


Figure 3.13.1 MAIN KEY STRUCTURE

The Keypad Interface is a peripheral controller, which can be used for scanning external keypad matrices with up to 8 rows and 8 columns (that is 64 standard keys). By adding an additional row of keys connected to ground the number of keys can be extended by up to 8 keys. This results in a maximum number of 72 keys to be identified by the Keypad Interface Controller.

The Keypad Scan Module reduces the number of interrupts and polling through the processor and therefore reduces the power consumption. The module is able to debounce and scan the external keypad matrix automatically without any software intervention. After debouncing it generates an interrupt. The interface controller contains information about the key (or key combination) that was pressed and how long it was pressed.

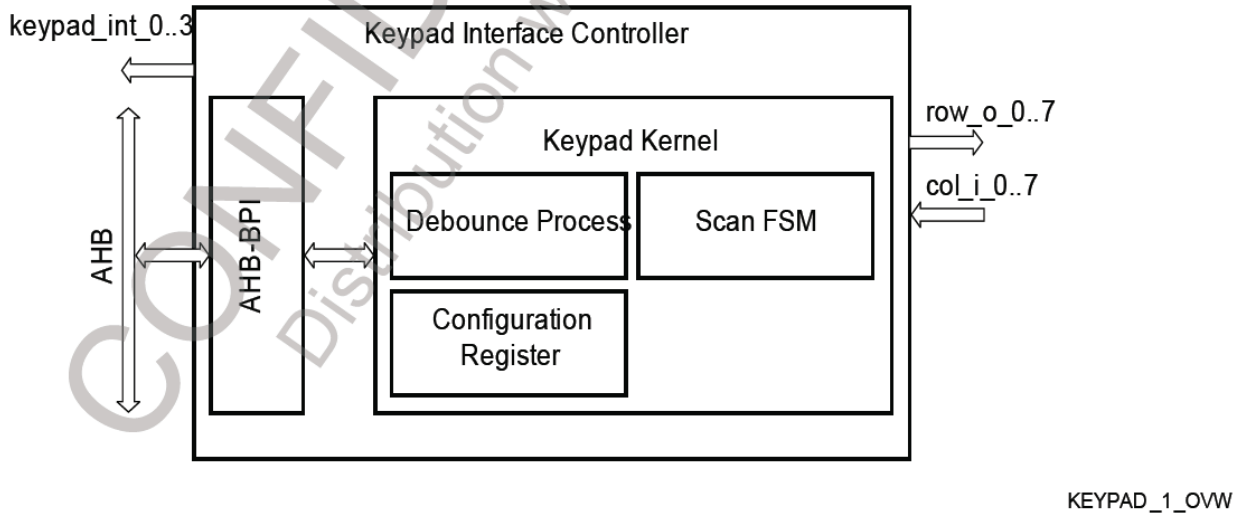


Figure 3.13.1 Block Diagram and System Integration of the KPD

Features of the Keypad Interface Controller

- Synchronous to bus
- 32 bit AHB bus interface
- 32.768 kHz sample clock
- Debouncing process (0 to 100 ms, 10 ms resolution) duration programmable by controller
- Module sends an interrupt, whenever a change occurs
- Up to 8 rows and 8 columns of a standard keypad matrix possible
- Up to 8 additional keys connected to ground possible
- Pressed key (or combination of pressed keys) and duration (0 to 1 s, 10 ms resolution) stored within keypad registers
- Rescan (0 to 100 ms, 10 ms resolution) to determine that pressed key(s) still the same.

3.14 Audio Front-End

3.14.1 Functional Overview

The audio front-end of X-GOLD™215 offers the digital and analog circuit blocks for both receive and transmit audio operation, from a mobile phone perspective (called audio-in and audio-out subsequently). It features a high-quality, stereo digital-to-analog path with amplifier stages for connecting acoustic transducers to X-GOLD™215. In audio-in path the supply voltage generation for electret microphones, a low-noise amplifier and analog to digital conversion are integrated in X-GOLD™215. A more detailed functional description will be given in the following sections.

The audio front-end itself can be considered to be organized in three sub-blocks:

- Interface to processor cores (TEAKLite® and - indirectly - ARM)
- Digital filters
- Analog part

The following figure shows an architecture overview of the Audio section.

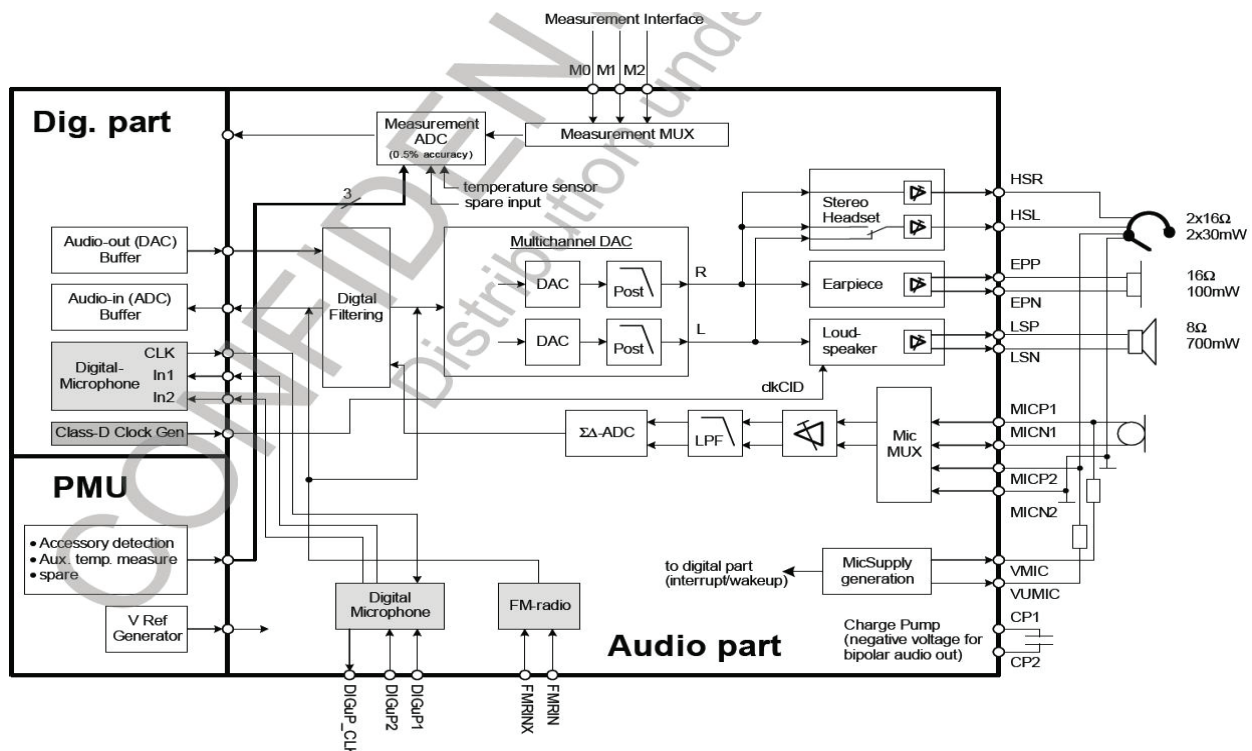


Figure 3.14.1 Audio Section Overview

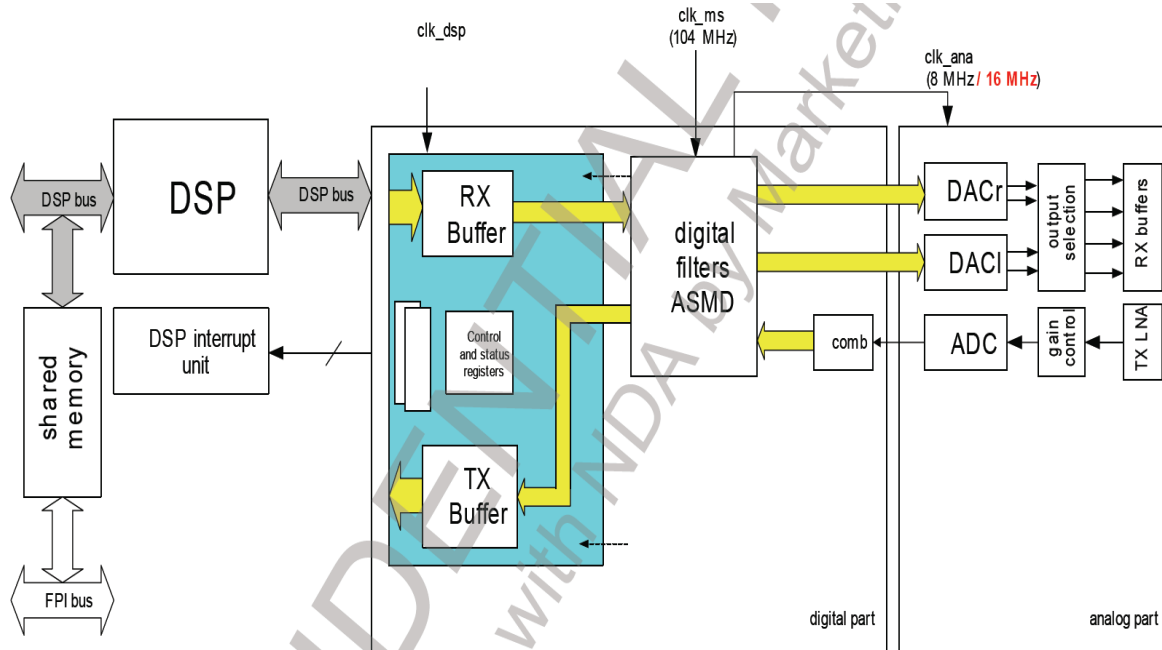


Figure 3.14.2 Overview of Clocking and Interfaces of Audio Front End

The audio front-end of X-GOLD™215 has the following major operation modes:

- Power-down: All analog parts are in power down and all clocks of the digital part are switched off.
- Audio mode: Digital decimation/interpolation filters are connected to the interface buffers and the analog part is enabled.

These major modes can be modified by certain control register settings.

- Due to the new gain settings in the TX path, the maximum input voltage is limited to 0.8 Vpp.
- In both voiceband paths, the value range for voice samples is confined to 97.5%, i.e. to [-31948, 31947] or [8334H, 7CCBH] in X-GOLD™215.
- On the TX path, 83% "1"s on the VTPDM line correspond to a 16-bit value of 7CCBH and 17% "1"s correspond to a 16-bit value of 8334H at the digital filter output. Thus the usable range is 66%. This range can be scaled to 100% by Firmware.
- The high-pass functions of the voiceband filters have to be implemented in firmware on TEAKLite®.

3.14.2 Digital Part

The digital part of the X-GOLD™215 audio front-end comprises an interface to the TEAKLite® bus, interfaces to the interrupt units of TEAKLite®, digital interpolation filters for oversampling digital-to-analog conversion, digital decimation filters for analog-to-digital conversion and an interface to the analog part of the audio front-end. For the digital microphone all the filtering is done in a dedicated hardware. The output sample stream is then fed in a duplicated ring buffer structure like the data from the analog microphone path (after A/D conversion and subsequent digital filtering).

▪ Interpolation Filter

The interpolation path of the X-GOLD™215 audio front-end increases the sampling rate of the audio samples to the rate of the digital-to-analog converter. Because the input sampling rates can vary between 8 kHz and 47.619 kHz the filter characteristic and oversampling ratio can be adjusted to the respective sampling rate. The requirements for the interpolation filters depend on the sampling rate, because a sufficient out-of-band discrimination in the audio frequency band (20 Hz,...,20 kHz) has to be ensured.

▪ Decimation Filter

The digital decimation filter on X-GOLD™215 has two operating modes: 8 kHz output sampling rate and 16 kHz output sampling rate (or 16 kHz output sample rate and 16kHz bandwidth in case of doubled ASMD clock).

3.14.3 Analog Part

The analog part of the X-GOLD™215 audio front-end in audio-out direction consists of a stereo digital to analog converter (multi-bit oversampling converter) which transforms the output of the digital interpolation filter into analog signals. It is followed by the gain control/amplifier section. The DAC outputs can be switched to several output buffers. In audio-in section there is an input multiplexer which selects either one of two differential microphone inputs to be connected to the low-noise amplifier and analog pre-filter. The signals from the analog pre-filter are input to a second-order sigma-delta analog-to-digital converter. In addition there is a connection for FM-radio playing.

▪ Audio-out Part

The analog audio-out part consists of two multi-bit digital-to-analogue converters (DAC) and an output stage. The signal sources are switched to the output drivers in the output stage. The output drivers consist of: a) one mono, differential class-D Loudspeaker driver, b) one mono, differential Earpiece driver and c) one stereo, single-ended (with uni- or bipolar signals), Headset driver.

▪ Digital-to-analog converters

The multi-bit oversampling DACs of the X-GOLD™215 audio front-end convert the 16-bit data words coming from the digital interpolation filters to analogue signals.

▪ Output Amplifier

The different output buffers in X-GOLD™215 are driven by the outputs of the selection block. The differential earpiece driver can be used to drive a 16 Ω earpiece and works in differential. The two single ended headset drivers can be used to drive a 16 Ω headset. They can work unipolar mode, where an AC coupling of the headset might be needed, or can work also in bipolar mode. The differential loudspeaker driver can be used to drive a 8 Ω loudspeaker. As it is a class-D amplifier the needed suppression of the higher harmonics of the switching signals

has to be achieved by the external circuitry. The buffers are designed to be short circuit protected.

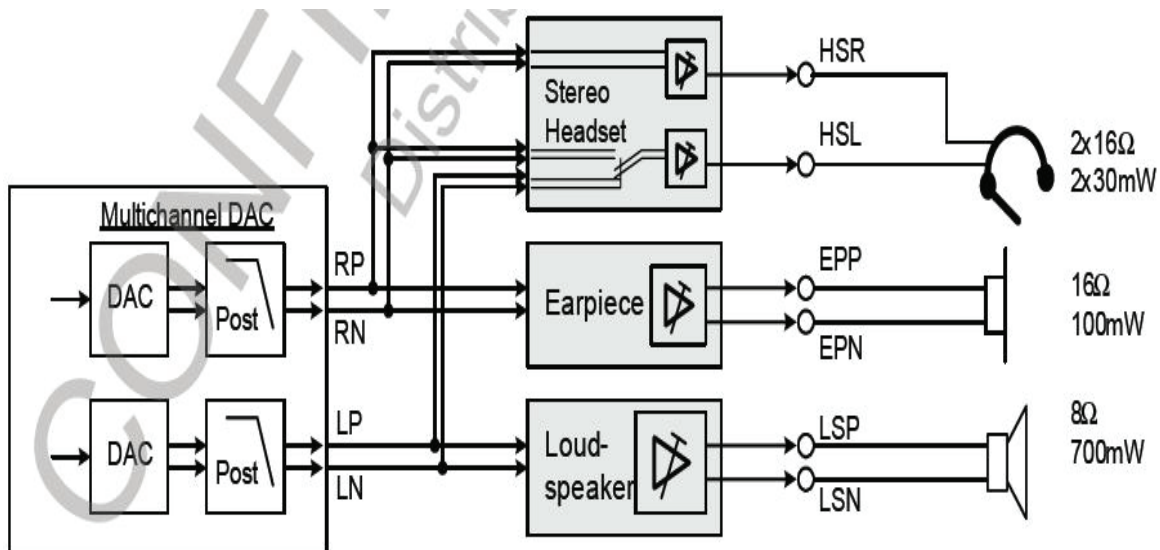


Figure 3.14.3 Switching for R/L DACs onto Buffers

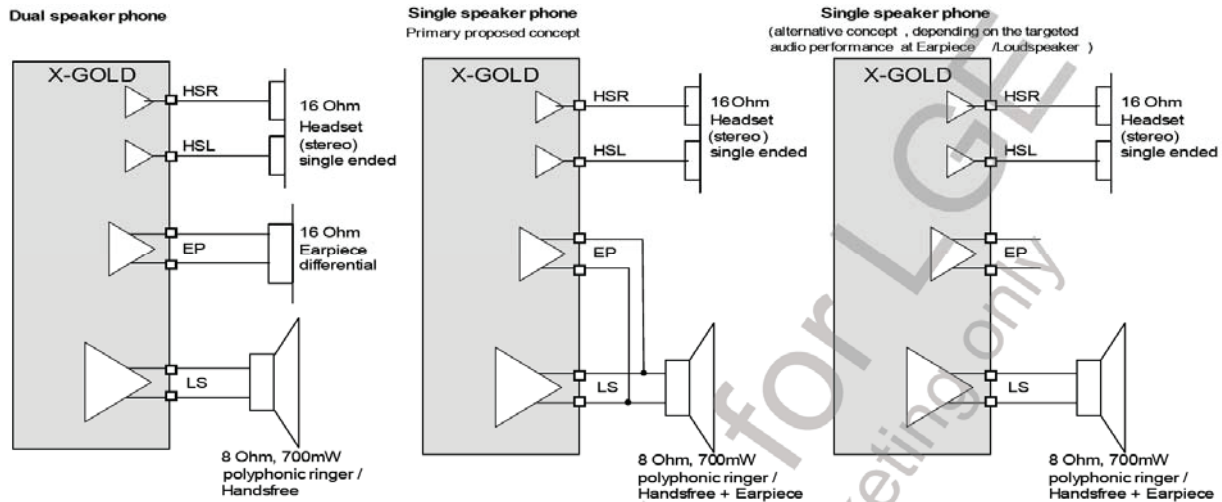


Figure 3.14.4 Different Application Scenarios

In order to achieve the single-speaker concept by parallel connection of Earpiece and Headset amplifier the Earpiece amplifier have to sustain the up to 5 V voltage of the class-D amplifier.

▪ Audio-in Path

The audio-in path of X-GOLD™215 provides two differential microphone input sources, MIC1 and MIC2.

- The inputs for microphone MIC1 are MICP1 and MICN1.
- The inputs for microphone MIC2 are MICP2 and MICN2.

The audio-in path consists of an input selector, a low noise amplifier and following pre-filter with gain control, a second order $\Sigma\Delta$ -converter and a digital decimation filter. It supports both standard GSM (bandwidth 3.5 kHz) and wideband (bandwidth 7 kHz) speech bands.

The differential input signal from the microphone first passes a low noise amplifier and following pre-filter and an anti-aliasing pre-filtering stage achieving and overall variable gain ranging from 0 dB to +39 dB.

The signal is then modulated by a second order $\Sigma\Delta$ -converter which is clocked with the same clock rate as the digital to analog converters. The $\Sigma\Delta$ -converter delivers a 1-bit pulse density modulated data stream at a rate of 2 MHz to the digital decimation filter which reduces the rate to 8 kHz or 16 kHz, depending on the current mode.

To improve SNR the sample frequency can be doubled in dedicated modes and the modulated data stream is 4MHz instead of 2 MHz.

▪ Microphone Supply

X-GOLD™215 has a single ended power-supply concept for electret microphones:

For both modes a minimal load capacitance of t.b.d. nF is necessary to guarantee stable operation of the buffer.

The maximal load capacitance must not exceed t.b.d. nF.

2 microphone supplies VMIC and VUMIC are available. The supply VUMIC has a ultra-low-power mode, where the current consumption is minimum, whilst at the same time the noise performance is reduced.

For this purpose the VUMIC is directly supplied out of the VMIC regulator, the Mic-Buffer can be switched off and only the quiescent current of the VMIC regulator is present. This mode can be used to supply a headset and allow accessory detection with highly reduced current consumption For normal operation the supply can be switched to normal operation mode with improved noise performance. In case of an digital microphone VMIC can be used for supplying this microphone.

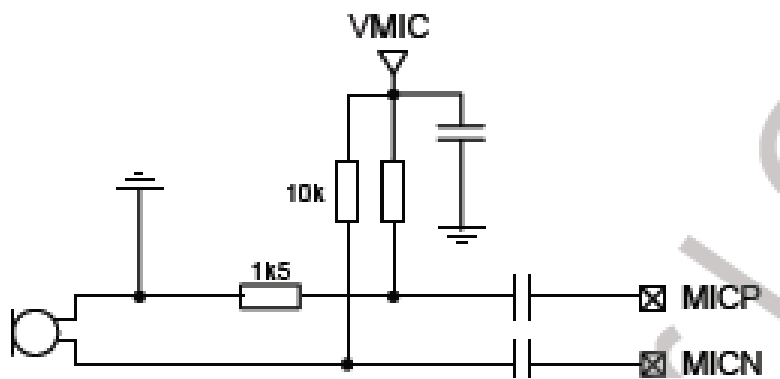


Figure 3.14.5 Typical Microphone Supply Generation (alternative)

3.15 Camera Interface

3.15.1 PMB8815 Camera Interface

The Camera Interface (CIF) represents a complete video and still picture input interface (see Figure 3.15.1). The CIF contains image processing, scaling, and compression functions. The integrated image processing unit supports image sensors with integrated $YCbCr$ processing.

Scaling is used for downsizing the sensor data for either displaying them on the LCD, or for generating data streams for MPEG-4 compression. In general, $YCbCr$ 4:2:2 JPEG compressed images should use the full sensor resolution, but they can also be downscaled to a lower resolution for smaller JPEG files. Scaling also can be used for digital zoom effects, because the scalers are capable of up-scaling as well.

CIF

All data is transmitted via the memory interface to an AHB bus system using a bus master interface.

Programming is done by register read/write transactions using an AHB slave interface.

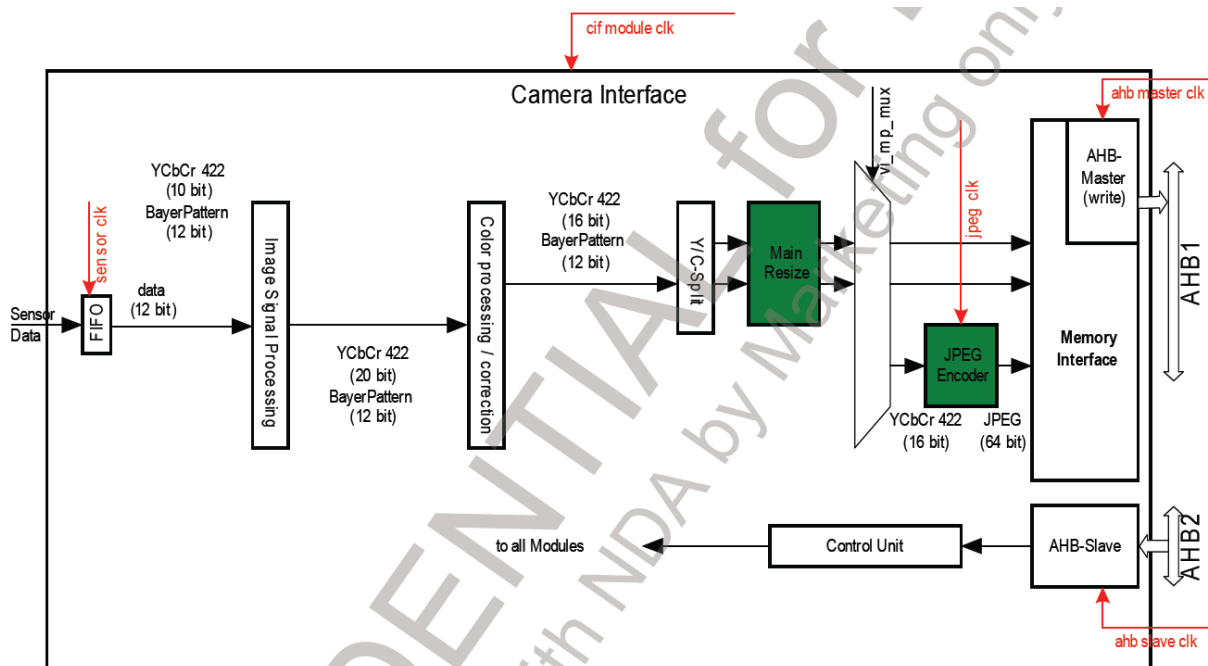


Figure 3.15.1 Block Diagram of Camera Interface

Functional Overview of CIF

The following list gives an overview over the CIF's functionality:

- 78 MHz system clock
- 78 MHz sensor clock
- 78 MHz JPEG encoder clock
- 32-bit AHB slave programming interface
- ITU-R BT 601 compliant video interface supporting $YCbCr$
- ITU-R BT 656 compliant video interface supporting $YCbCr$ data
- 8-bit camera interface
- 12-bit resolution per color component internally
- $YCbCr$ 4:2:2 processing
- Hardware JPEG encoder incl. JFIF1.02 stream generator and programmable quantization and Huffman tables
- Windowing and frame synchronization
- Continuous resize support
- Frame skip support for video (e.g. MPEG-4) encoding
- Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
- Programmable polarity for synchronization signals
- Luminance/chrominance and chrominance blue/red swapping for YUV input signals
- Maximum input resolution of 3 Mpixels (2048x1536 pixels)
- Main scaler with pixel-accurate up- and down-scaling to any resolution between 3 MP (2048x1536) and 32x16 pixel in processing mode
- Buffer in system memory organized as ring-buffer
- Buffer overflow protection for raw data and JPEG files
- Asynchronous reset input, software reset for the entire IP and separate software resets for all sub-modules
- Interconnect test support
- Semi planar storage format
- Color processing (contrast, saturation, brightness, hue)
- Power management by software controlled clock disabling of currently not needed sub-modules

3.16 KEY BACKLIGHT LED Interface

Key Backlight LED is controlled by switch (Q200). If KEY_BL_EN is high, Current is flowing from VBAT to LED. Then Light emitted from The LED.

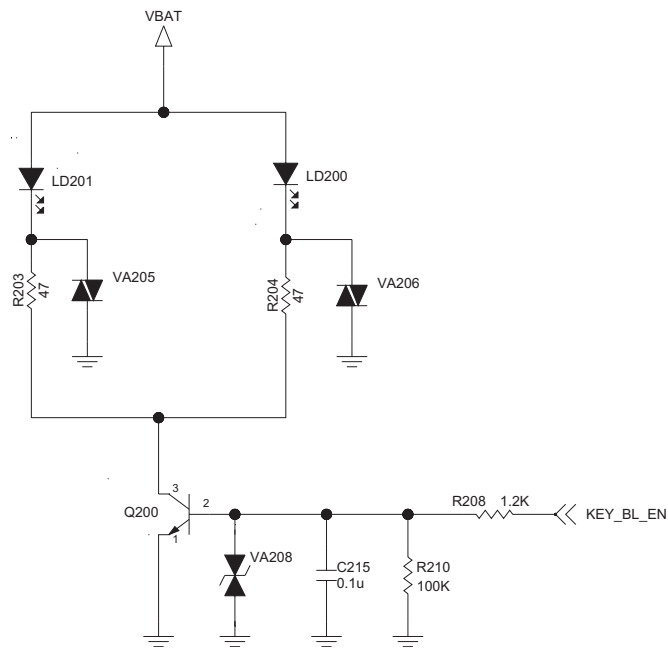


Figure 3.16.1 Key Backlight Block

4. TROUBLE SHOOTING

4.1 Trouble shooting test setup

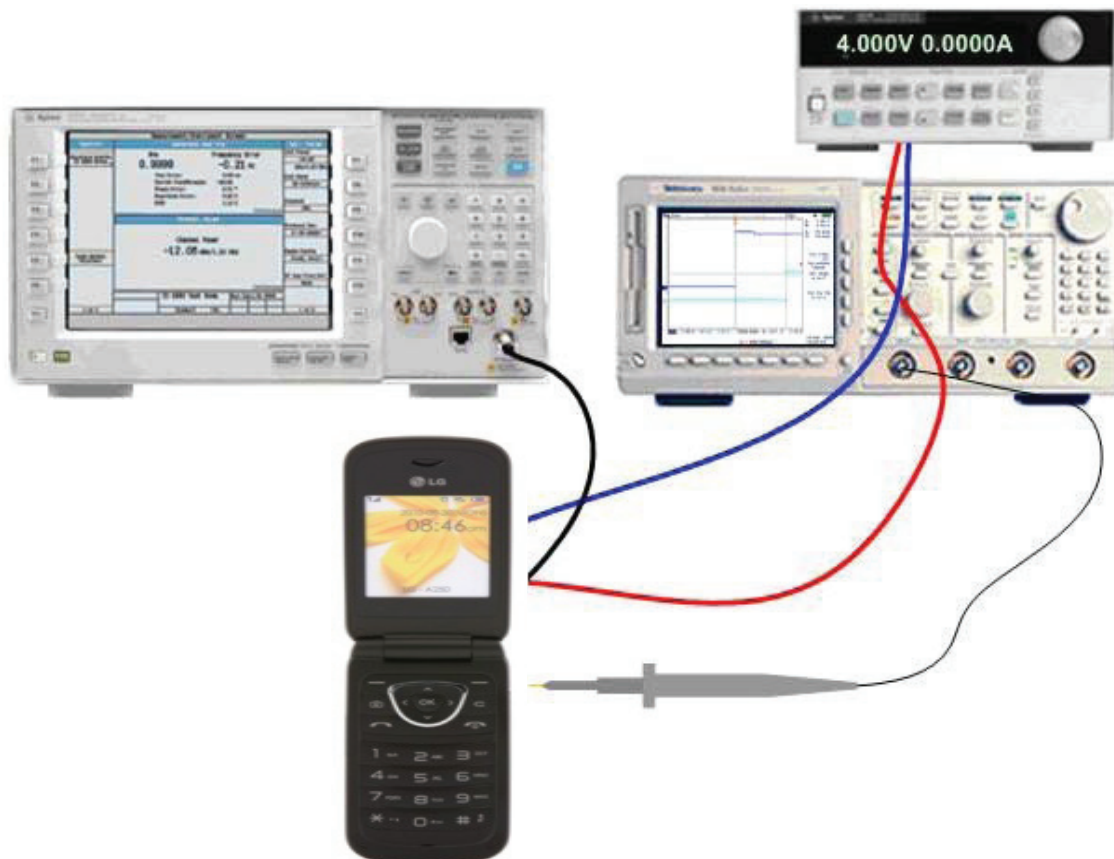


Figure 4.1.1 Equipment setup

Power on all of test equipment

- Connect PIF-UNION JIG or dummy battery to the DUT for power up.
- Connect mobile switch cable between Communication test set and DUT when you need to make a phone call.
- Follow trouble shooting procedure

4.2 RF Component

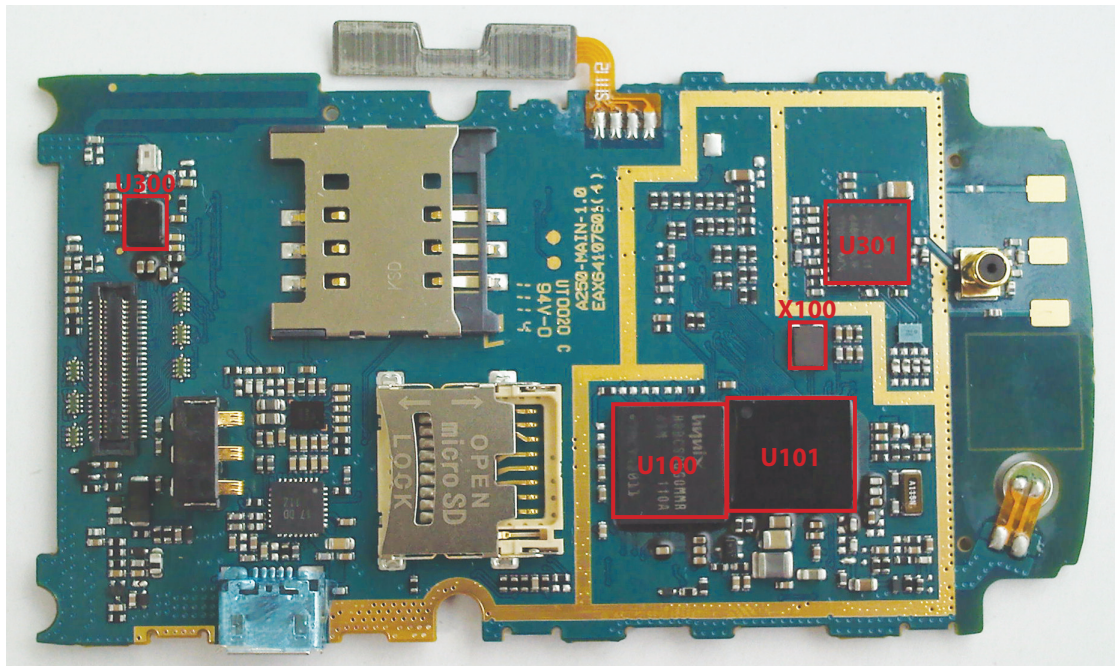
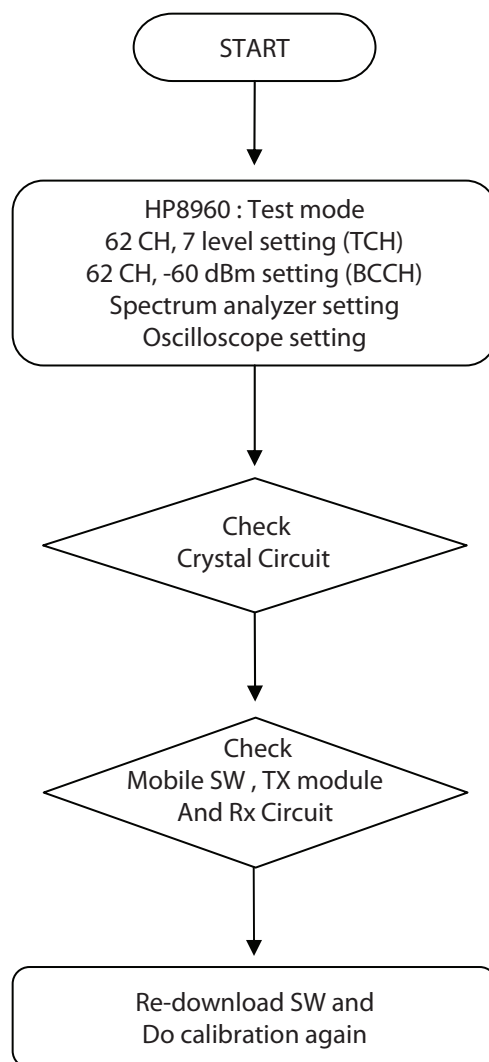


Figure 4.2 Main block

U301	RF Tx Module (SKY77550)
U100 (PMB8815)	Main Chip (AGR+NAND)
U100	MEMORY(1G NAND + 512M) H8BCS0QG0MMR-46M
X100	Crystal, 26MHz Clock
U300	Bluetooth (BCM2070, 0.4pitch)

4.3 RX Trouble

CHECKING FLOW



4.3.1 Checking Crystal Circuit

TEST POINT

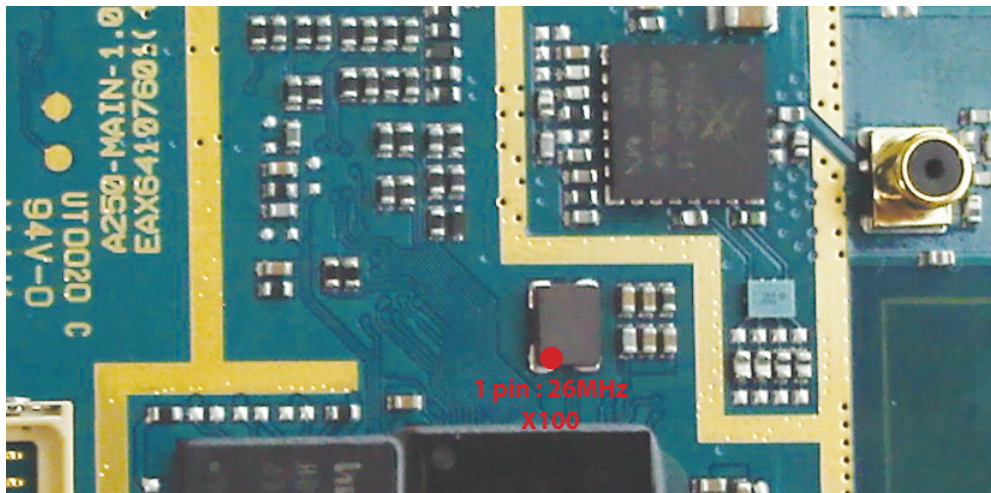
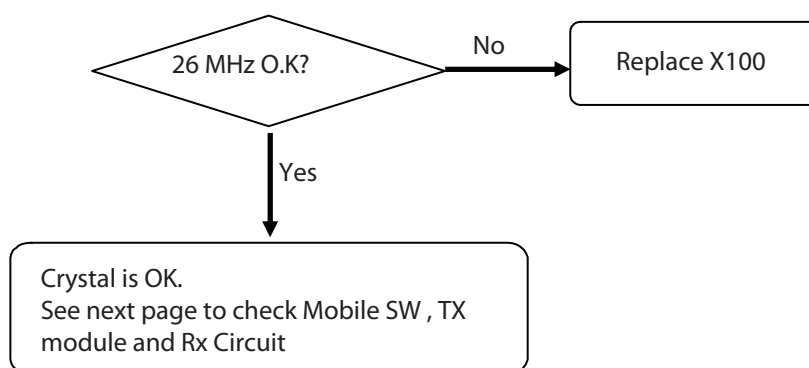


Figure 4.3.1 Main Crystal

CHECKING FLOW



CIRCUIT

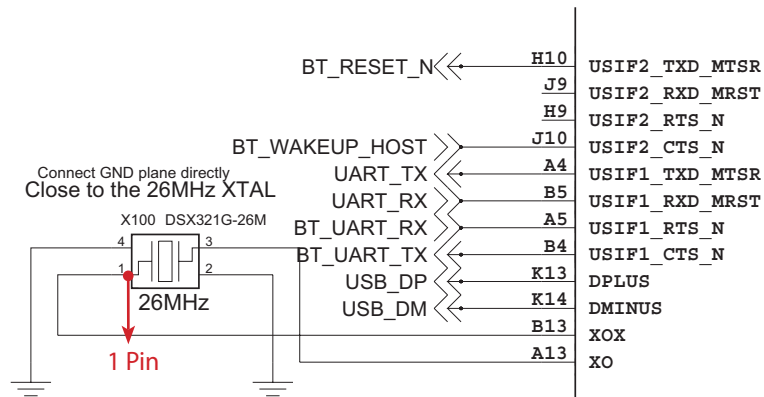


Figure 4.3.2 SIM 1 crystal circuit

WAVEFORM

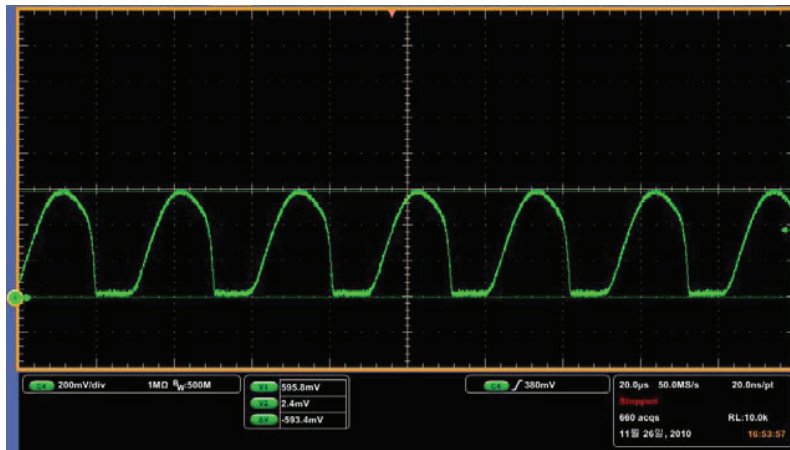


Figure 4.3.3 26MHz output waveform

4.3.2 Checking Mobile SW & FEM

TEST POINT

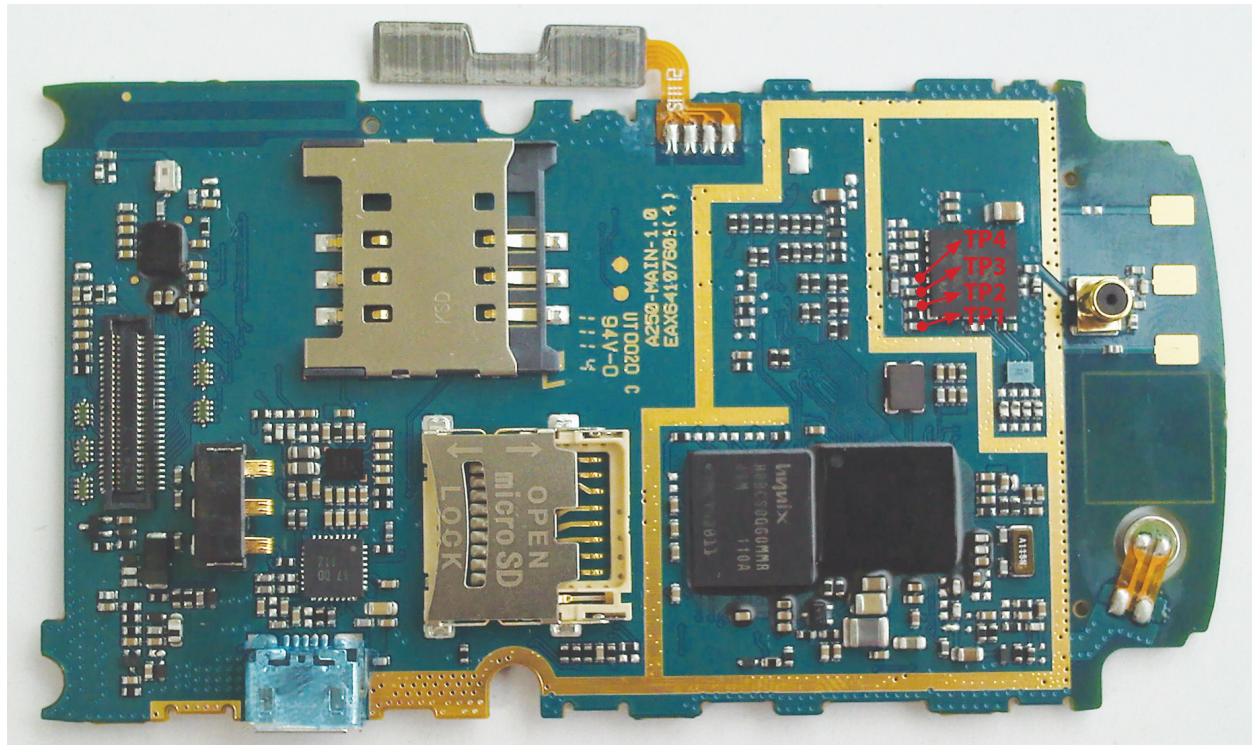


Figure 4.3.4 SIM 2 Mobile SW & FEM

4. TROUBLE SHOOTING

CIRCUIT

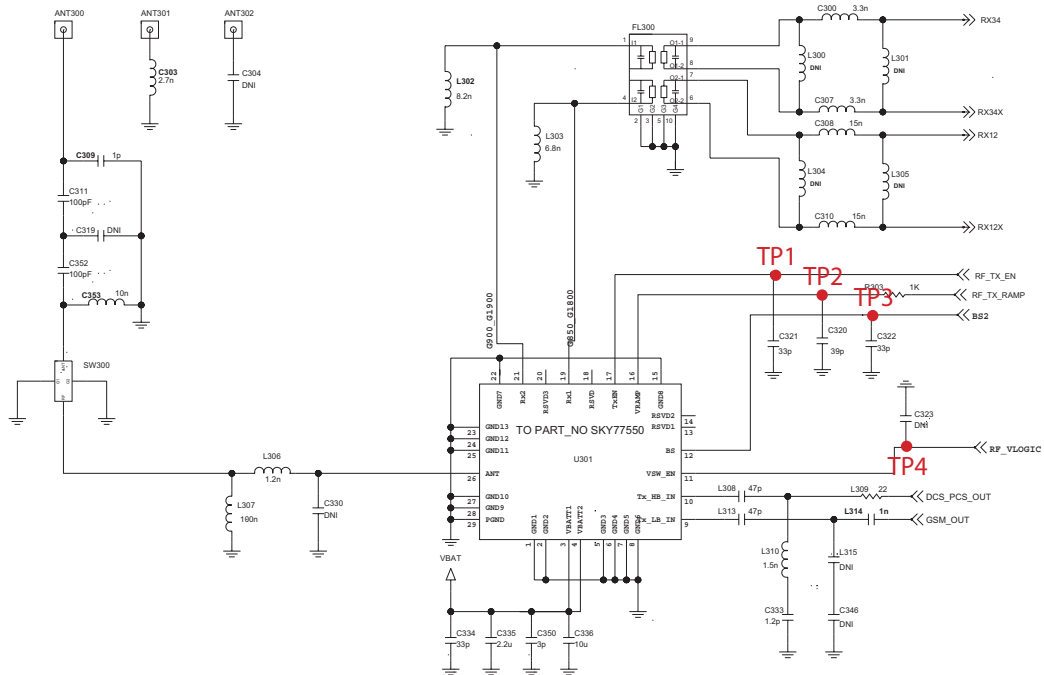


Figure 4.3.5 SIM1 Mobile SW & FEM circuit

CONTROL LOGIC

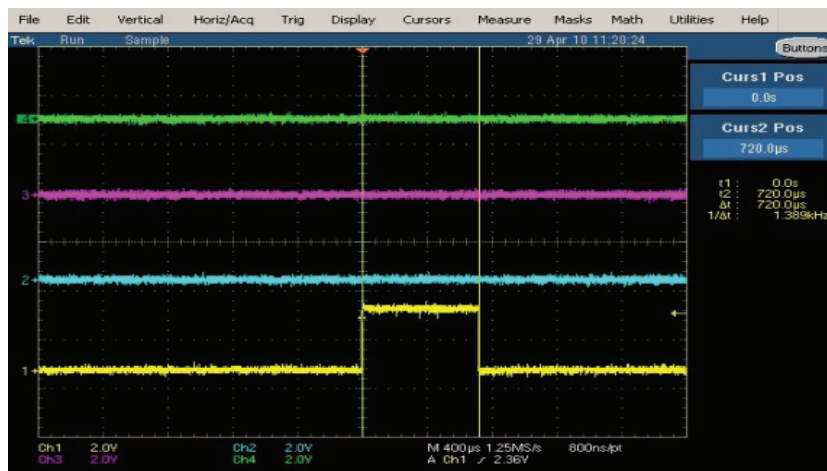
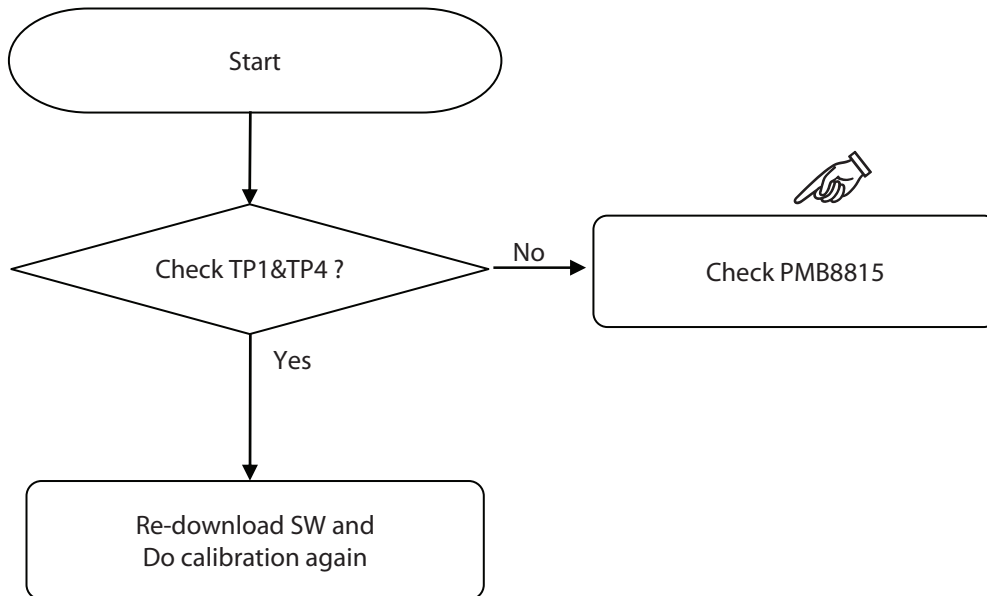


Figure 4.3.6 TP4 ~ TP6 Control Logic

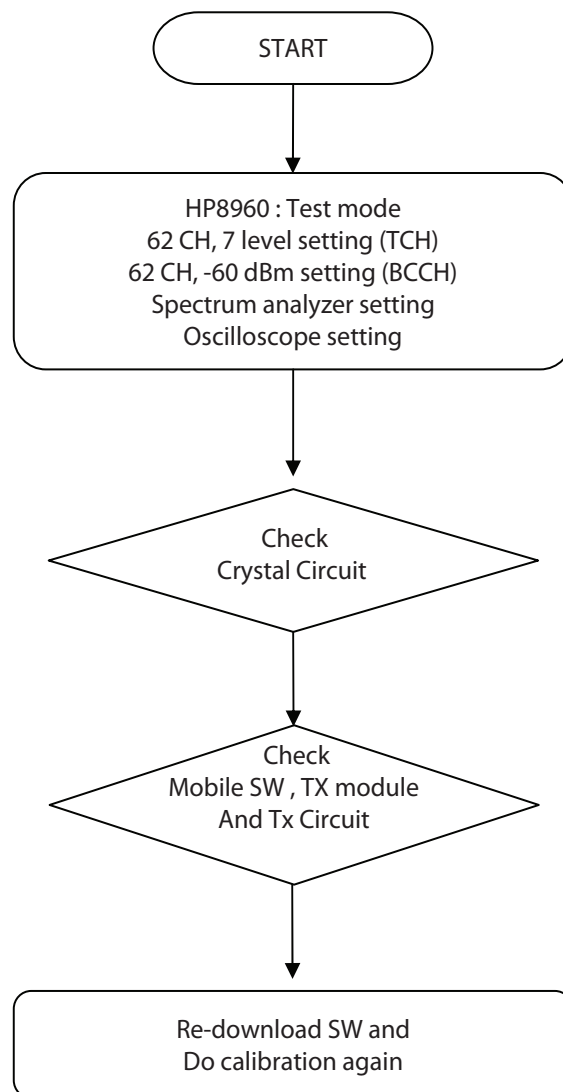
CHECKING FLOW



	TP4	TP1	TP3
MODE	RF_VLOGIC	RF_TX_EN	RF_BS
Standby	LOW	LOW	LOW
RX1	HIGH	LOW	LOW
RX2	HIGH	LOW	HIGH
TX_LB	HIGH	HIGH	LOW
TX_HB	HIGH	HIGH	HIGH

4.4 TX Trouble

CHECKING FLOW



4.4.1 Checking Crystal Circuit

TEST POINT

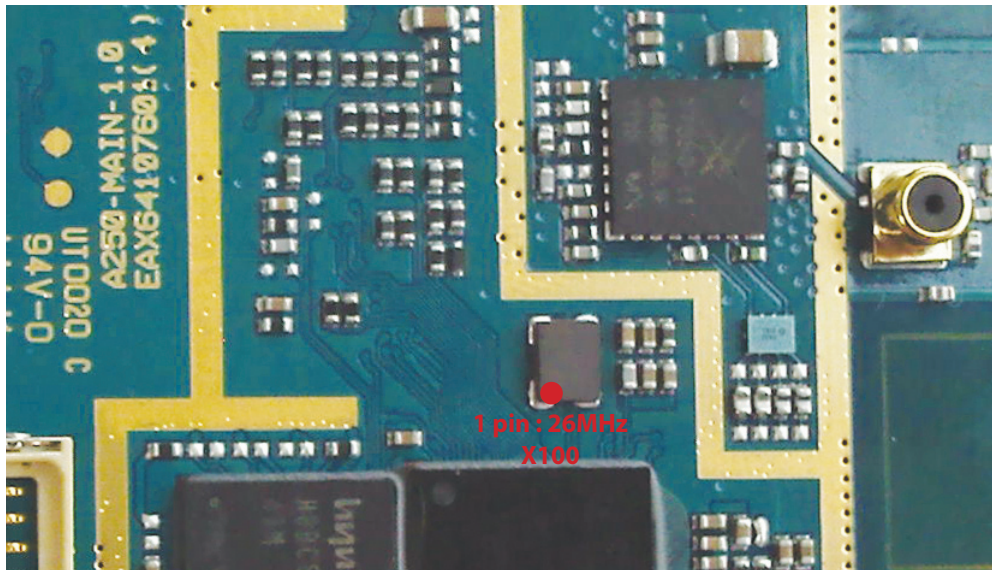
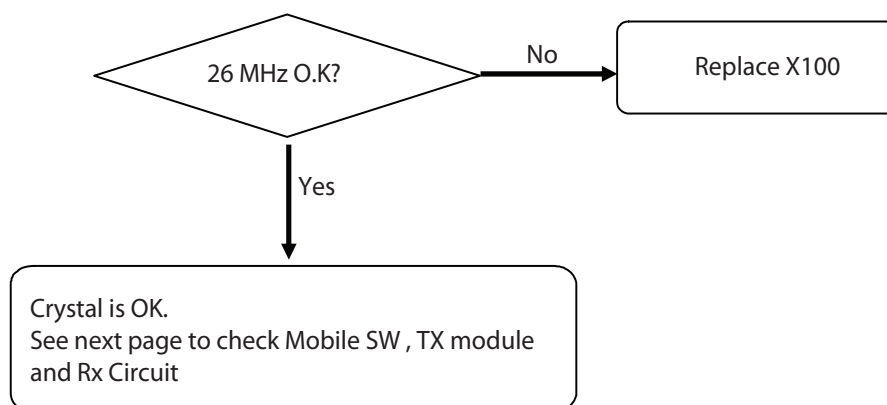


Figure 4.4.1 crystal unit

CHECKING FLOW



CIRCUIT

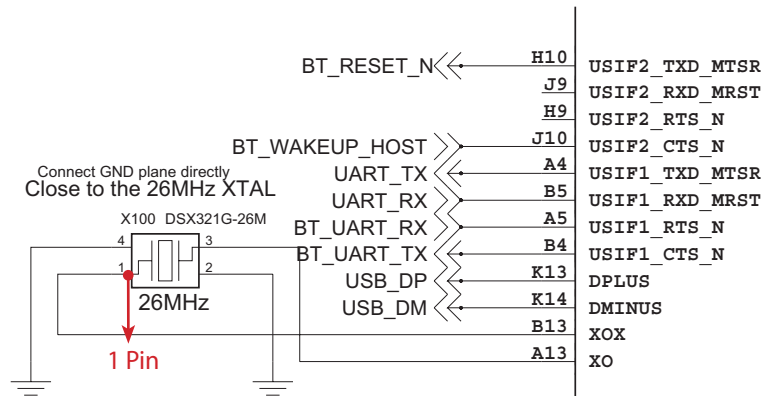


Figure 4.4.2 SIM 1 crystal circuit

WAVEFORM

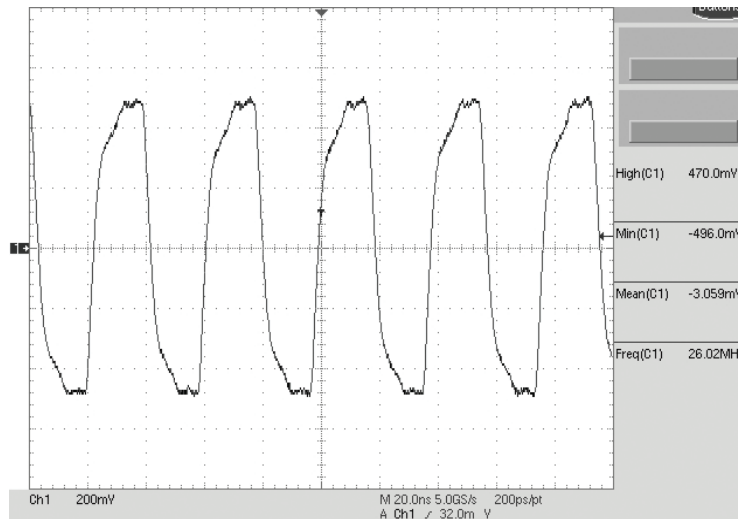


Figure 4.4.3 26MHz output waveform

4.4.2 Checking Mobile SW & TX Module

TEST POINT

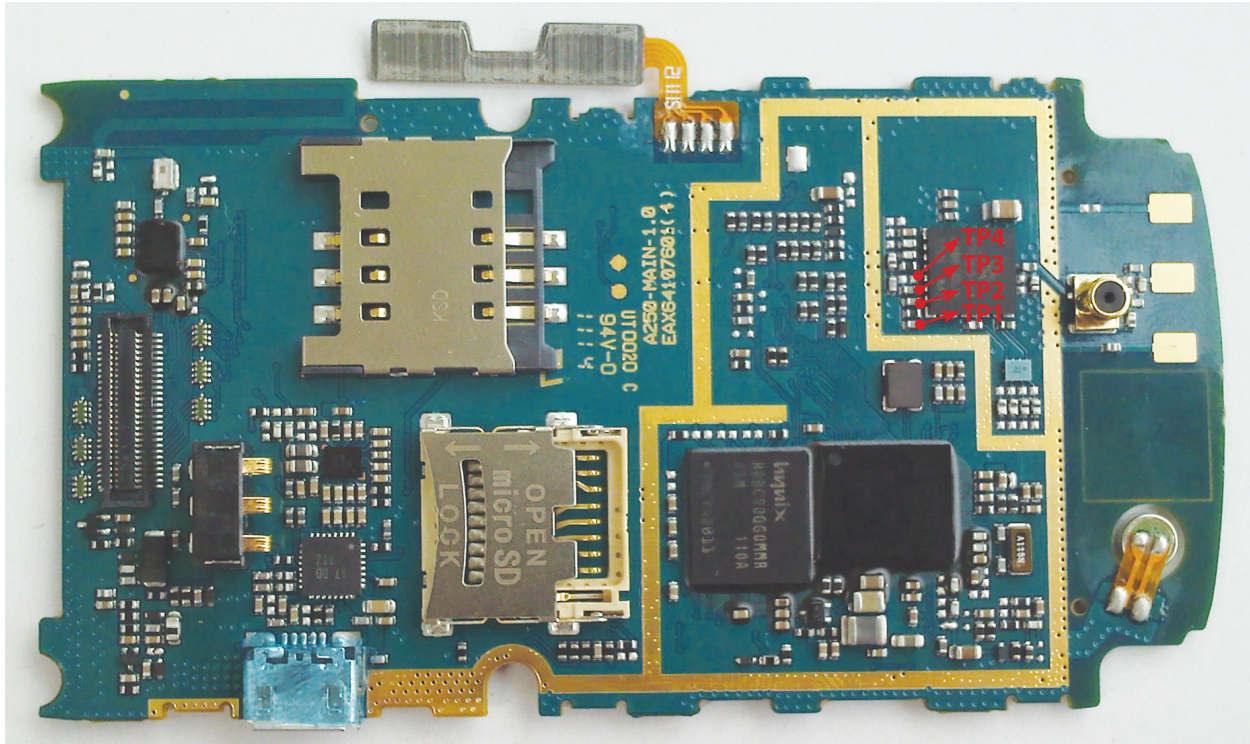


Figure 4.3.4 SIM 2 Mobile SW & TX Module

4. TROUBLE SHOOTING

CIRCUIT

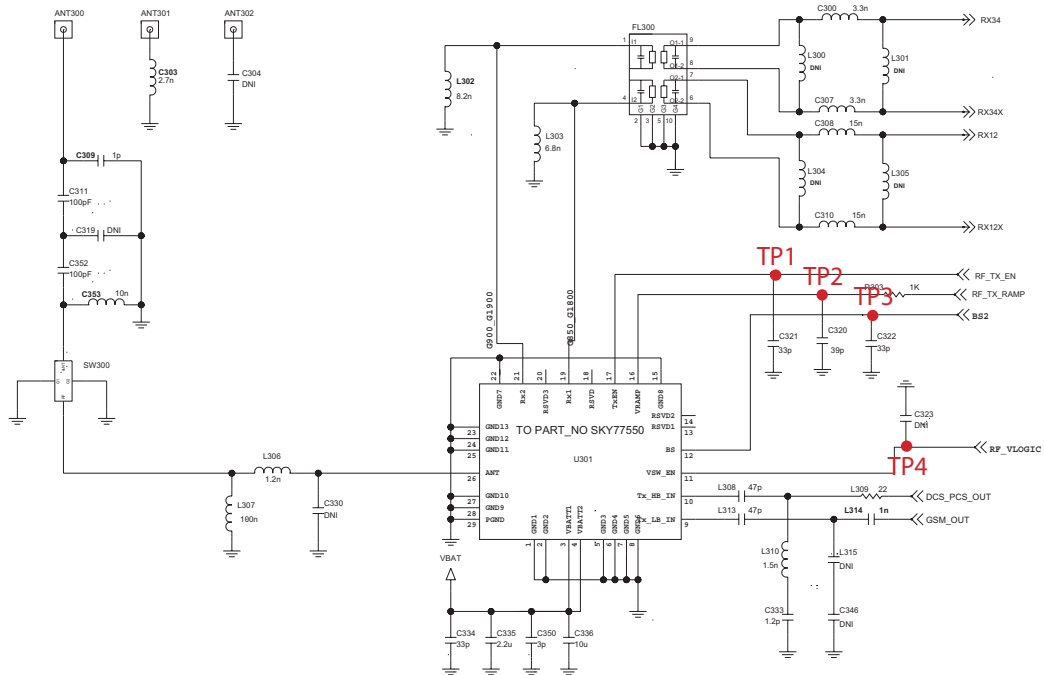


Figure 4.4.5 SIM1 Mobile SW & TX Module

CONTROL LOGIC

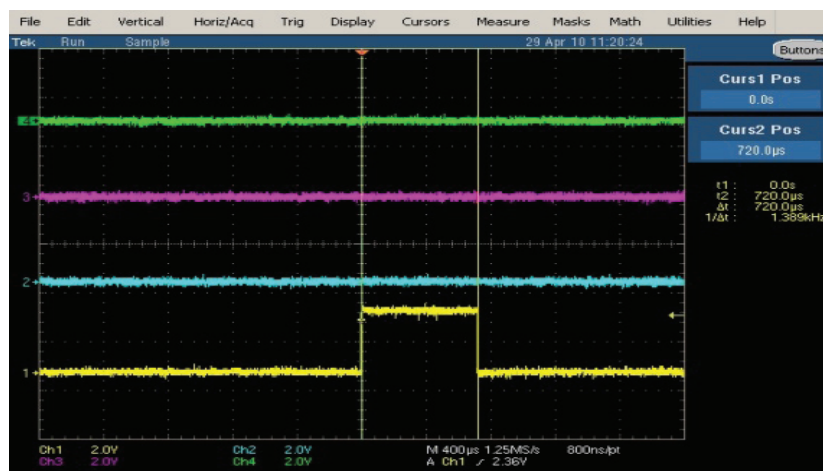
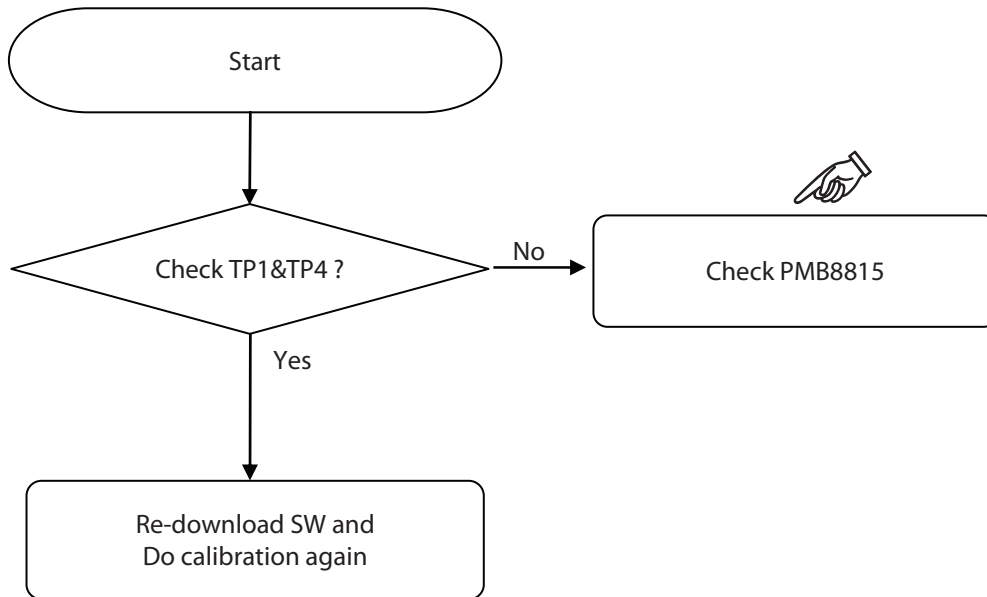


Figure 4.4.6 TP4 ~ TP6 Control Logic

CHECKING FLOW



	TP4	TP1	TP3
MODE	RF_VLOGIC	RF_TX_EN	RF_BS
Standby	LOW	LOW	LOW
RX1	HIGH	LOW	LOW
RX2	HIGH	LOW	HIGH
TX_LB	HIGH	HIGH	LOW
TX_HB	HIGH	HIGH	HIGH

4.5 Power On Trouble

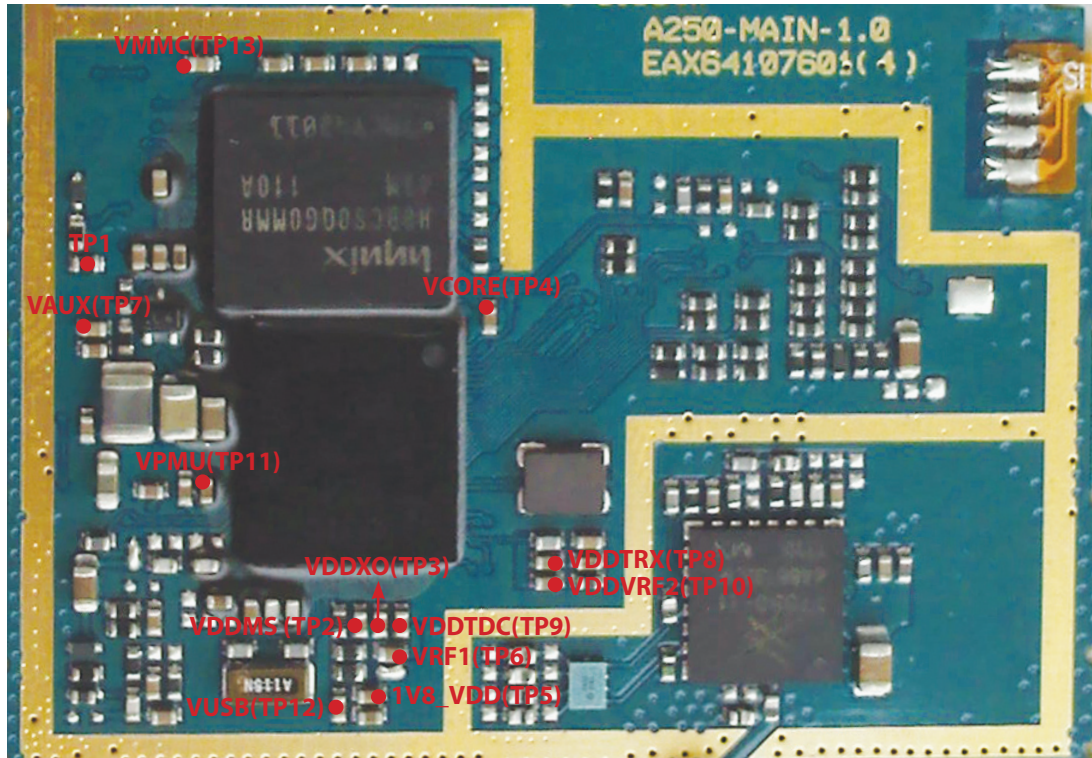


Figure 4.5.1

4. TROUBLE SHOOTING

CIRCUIT

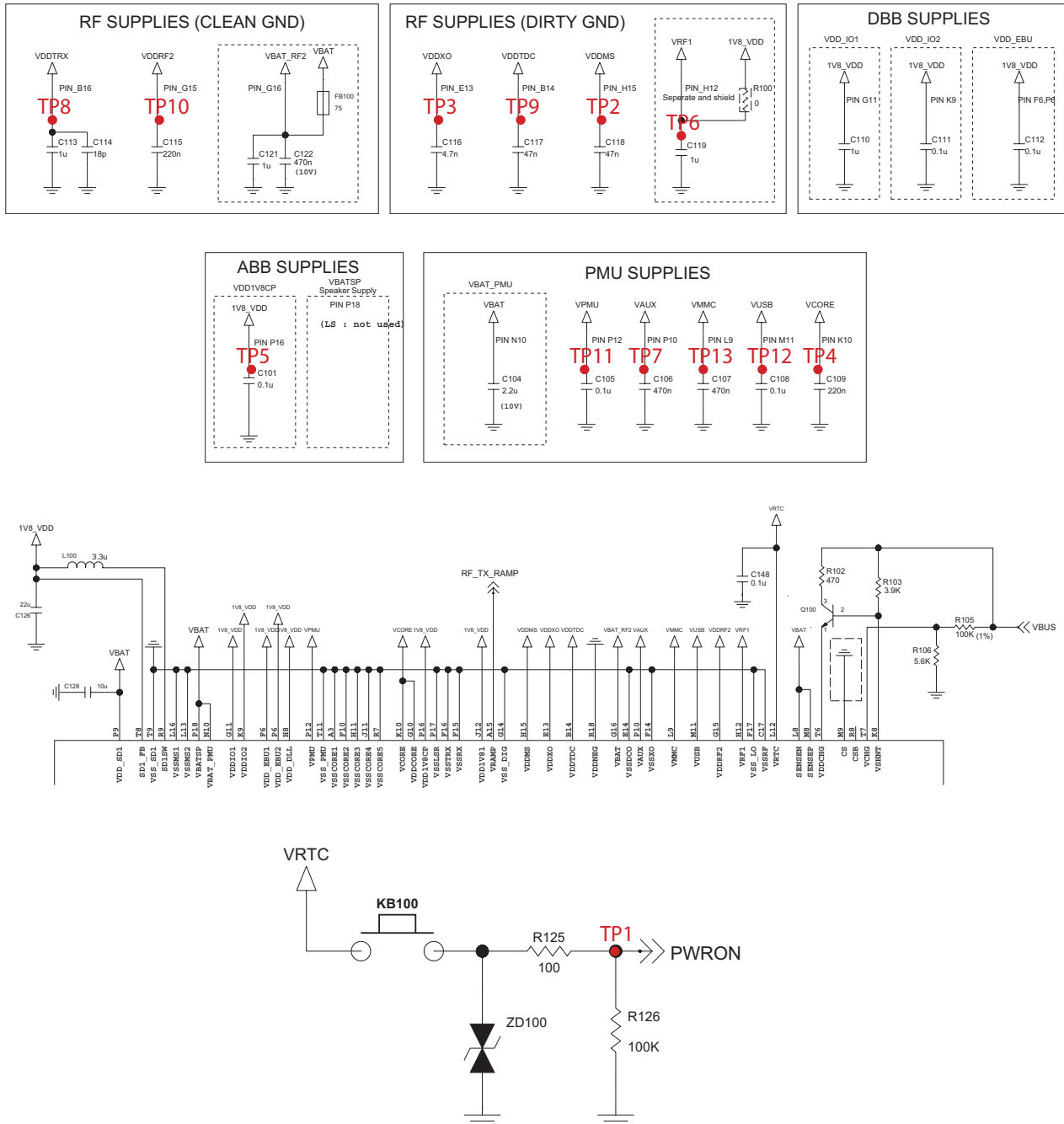
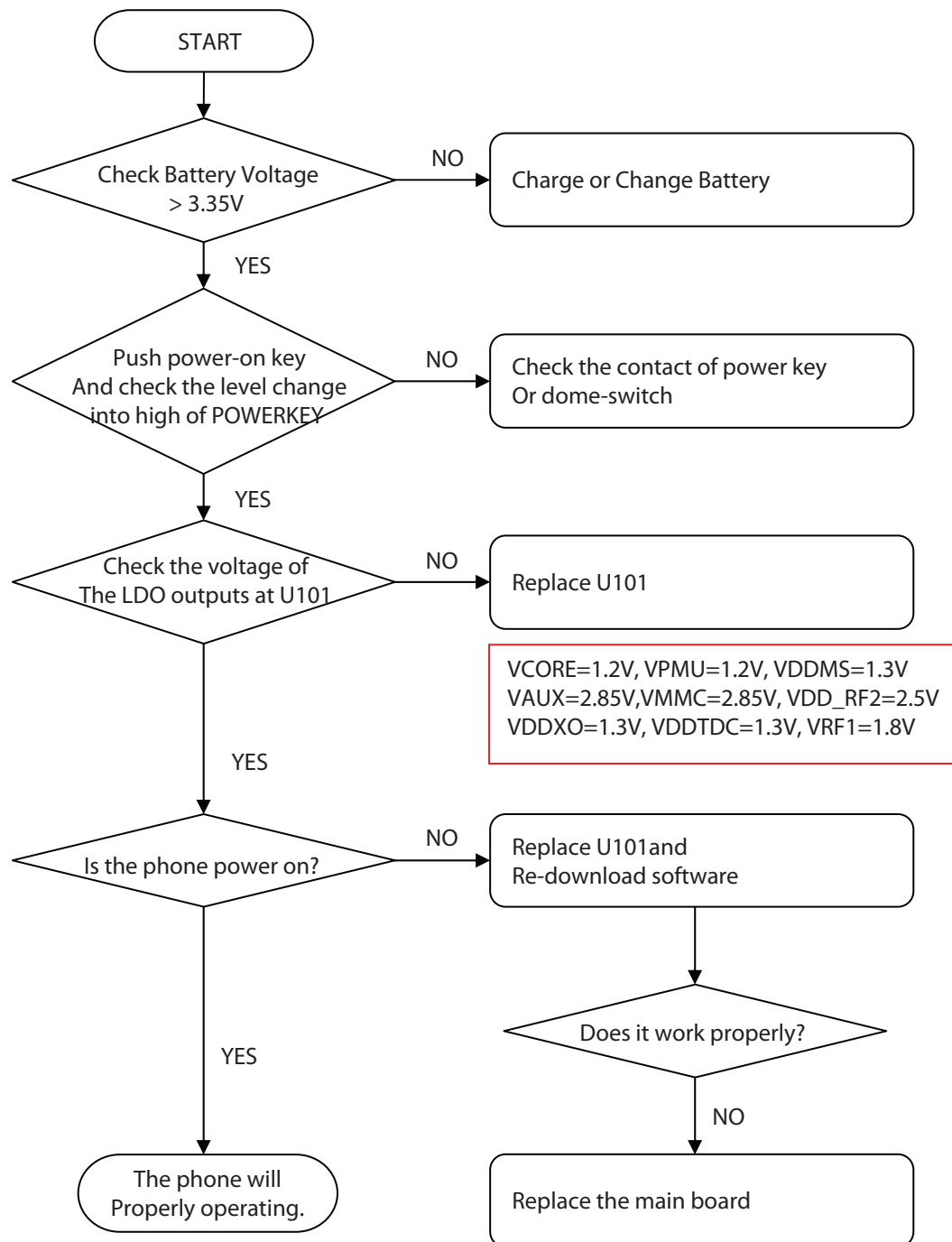


Figure 4.5.3 power block of LG-A258

CHECKING FLOW



4.6 Charging Trouble

TEST POINT

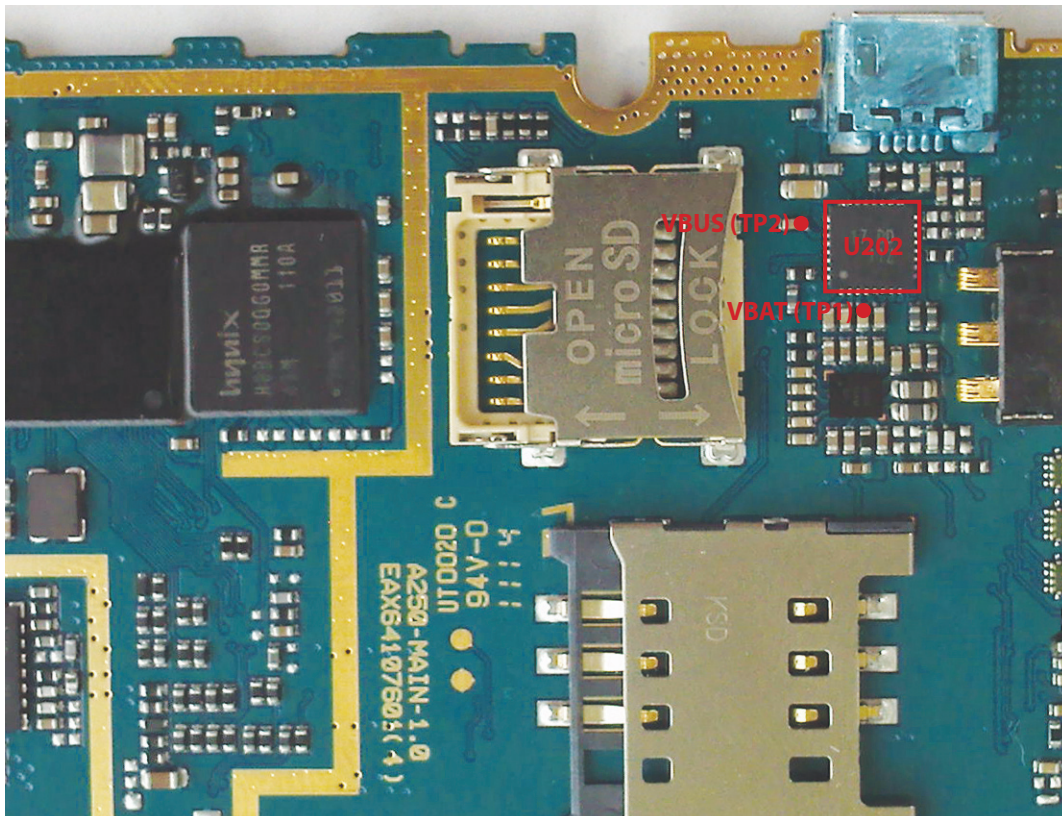


Figure 4.6.1

CIRCUIT

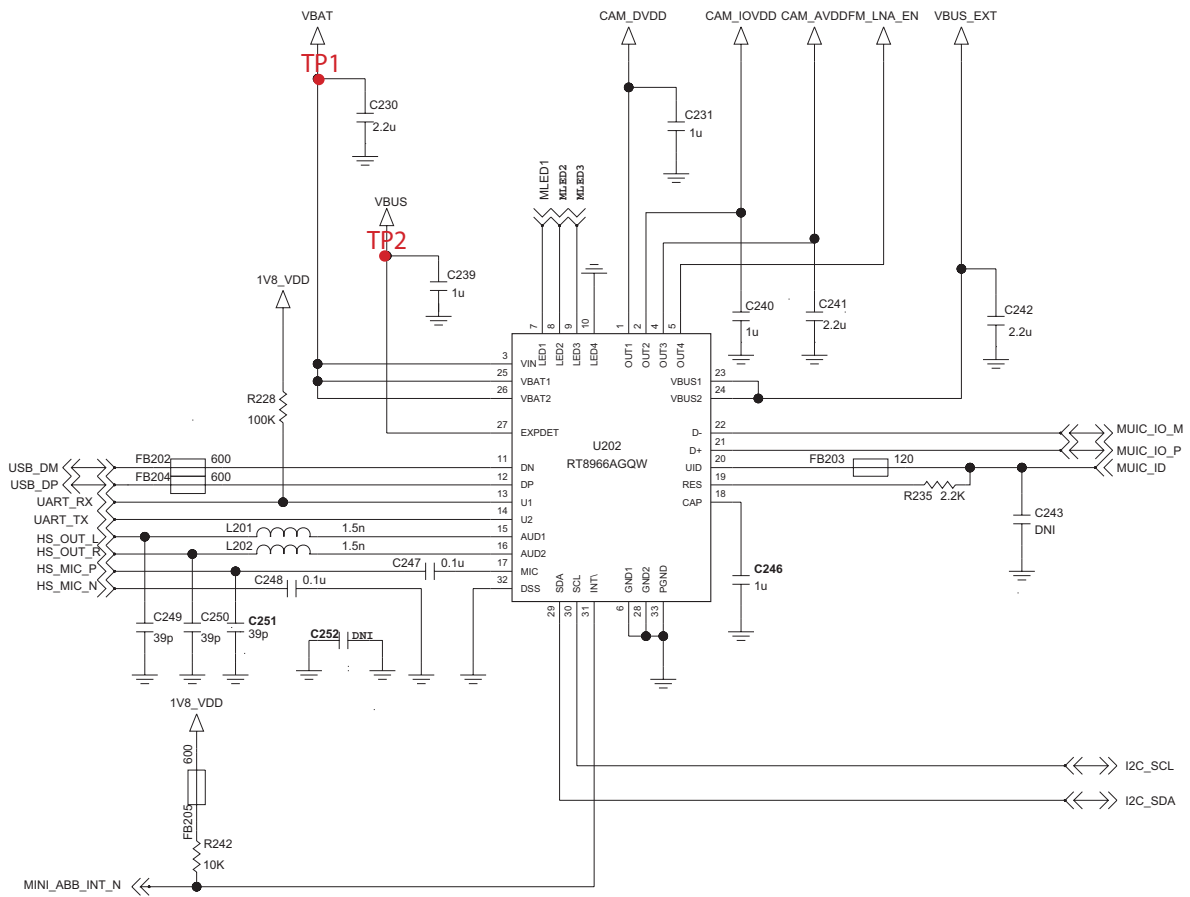
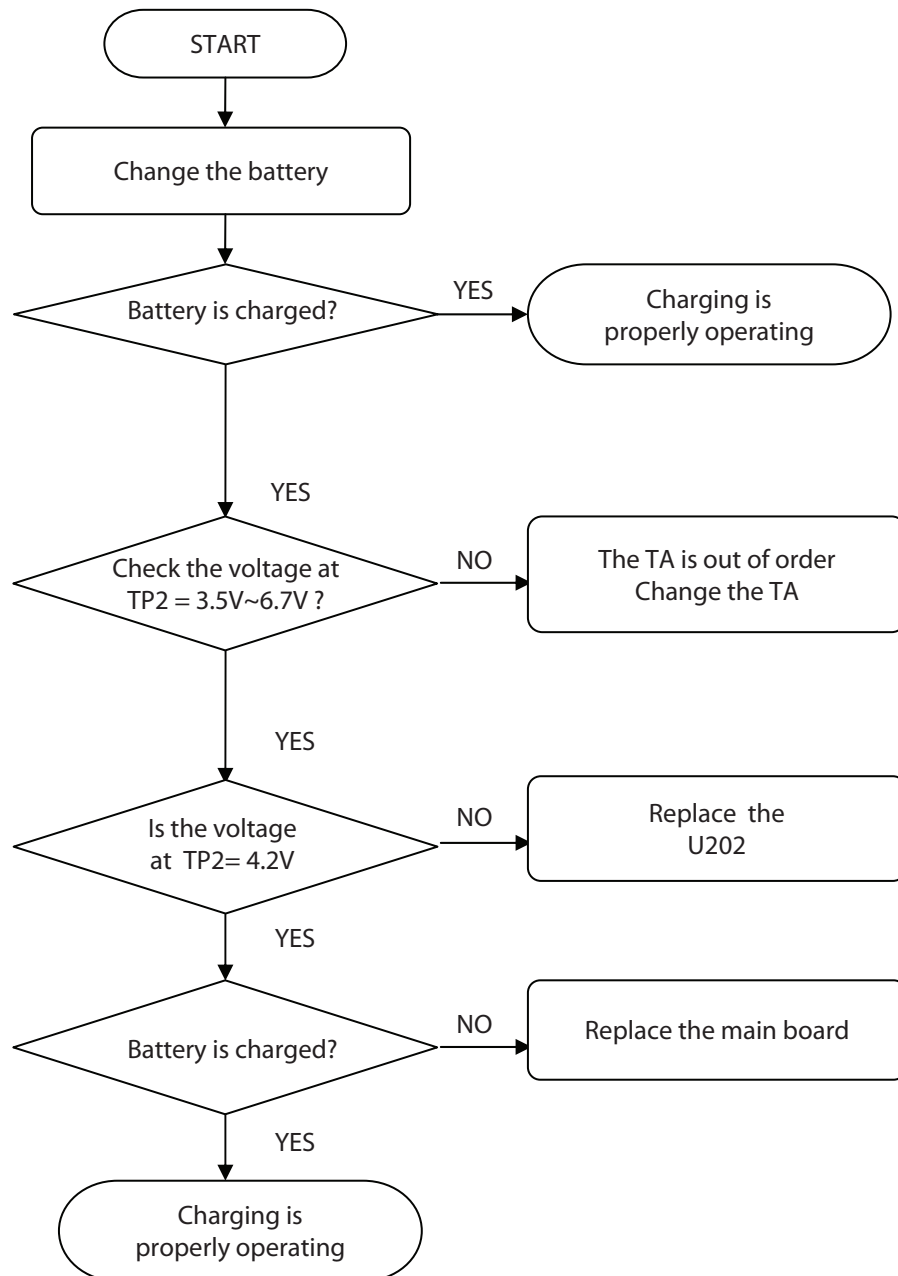


Figure 4.6.2

CHECKING FLOW



4.7 Vibrator Trouble

TEST POINT

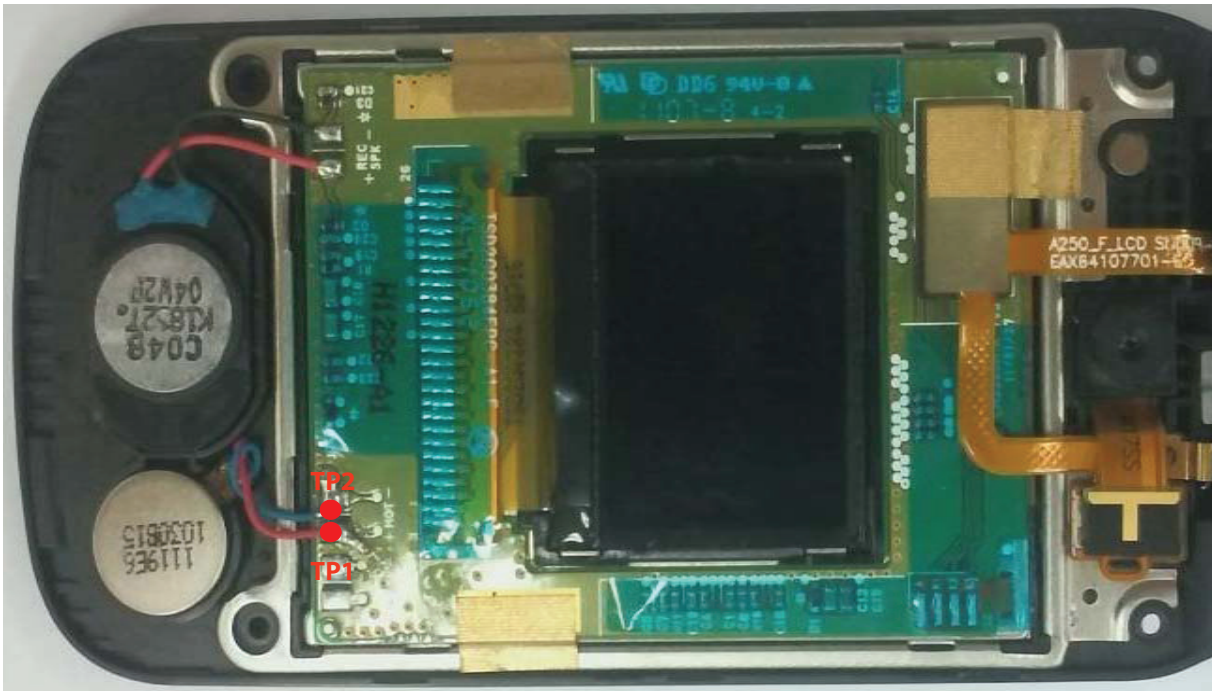


Figure 4.7.1

CIRCUIT

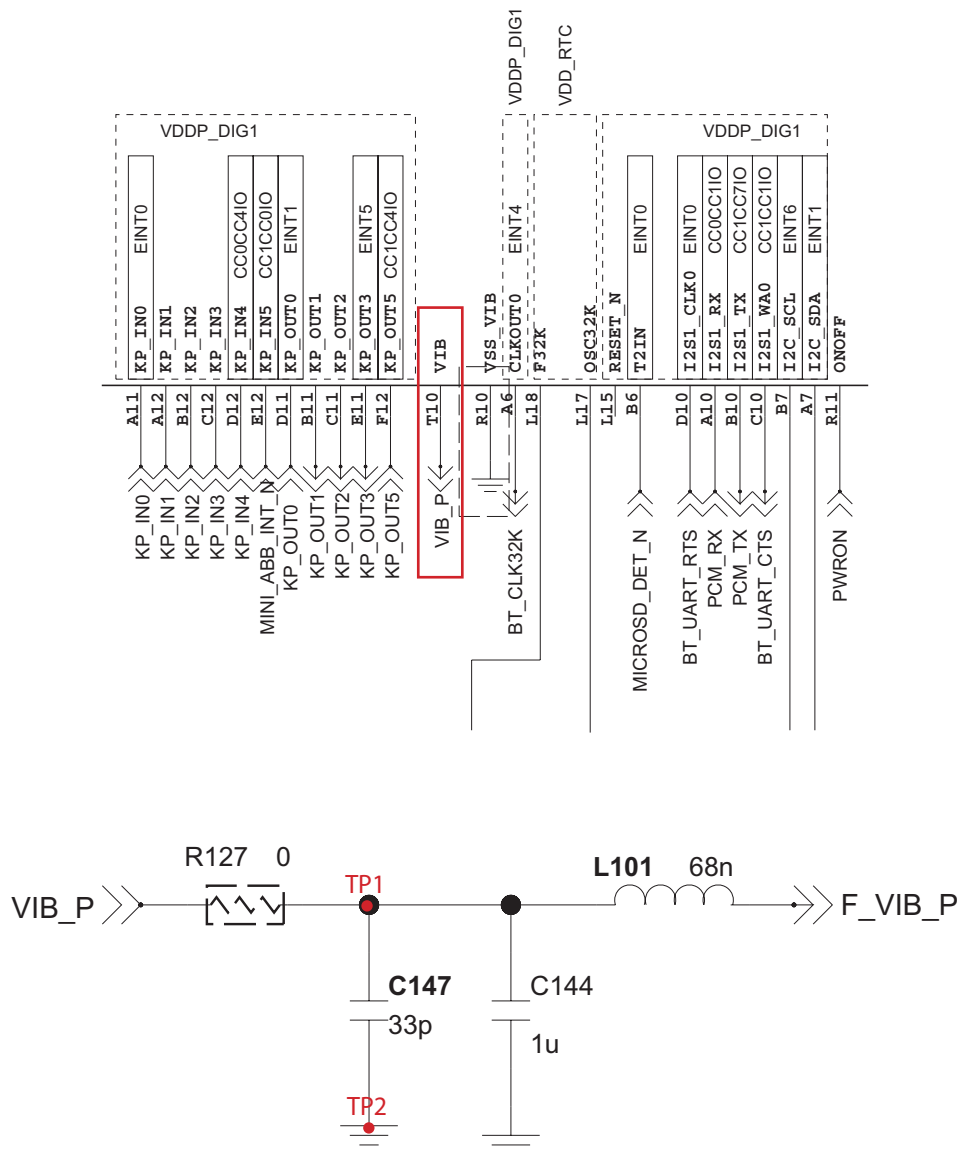
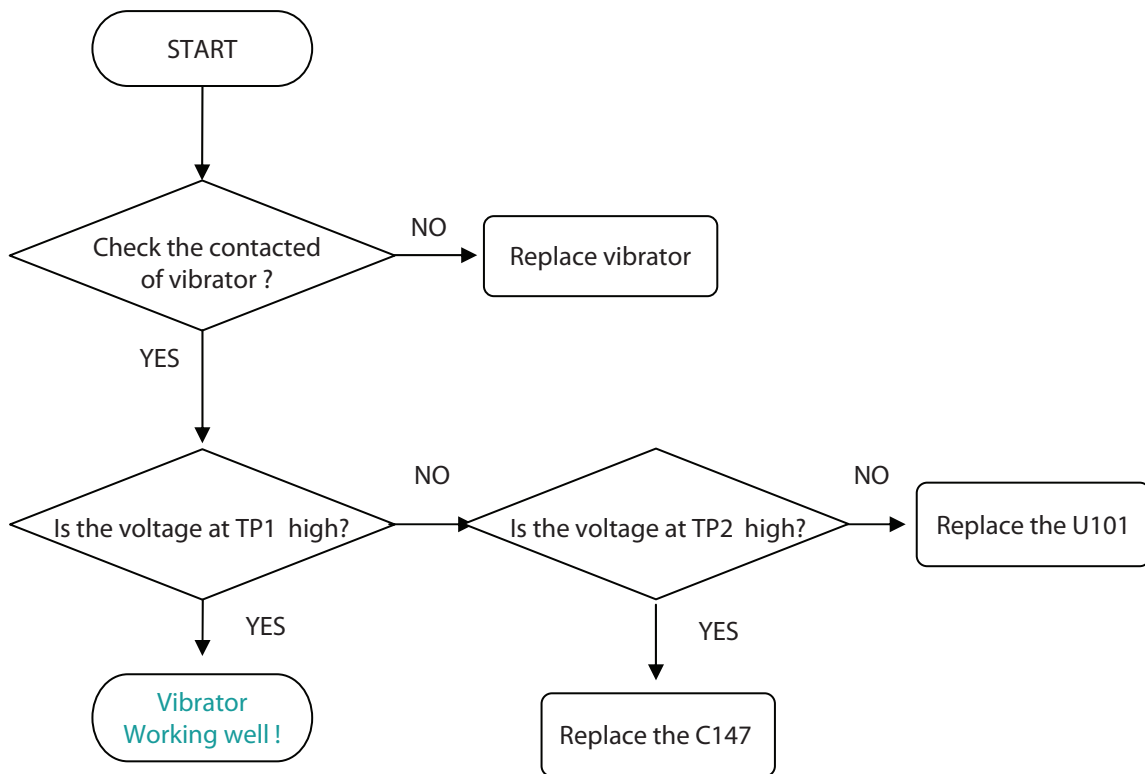


Figure 4.7.2

CHECKING FLOW

SETTING : Enter the engineering mode, and set vibrator on at vibration of BB test menu



4.8 LCD Trouble

TEST POINT

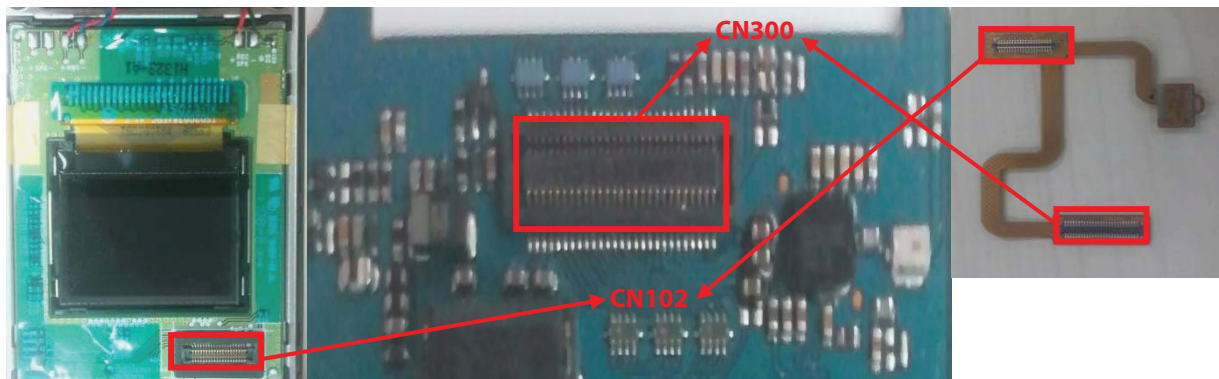
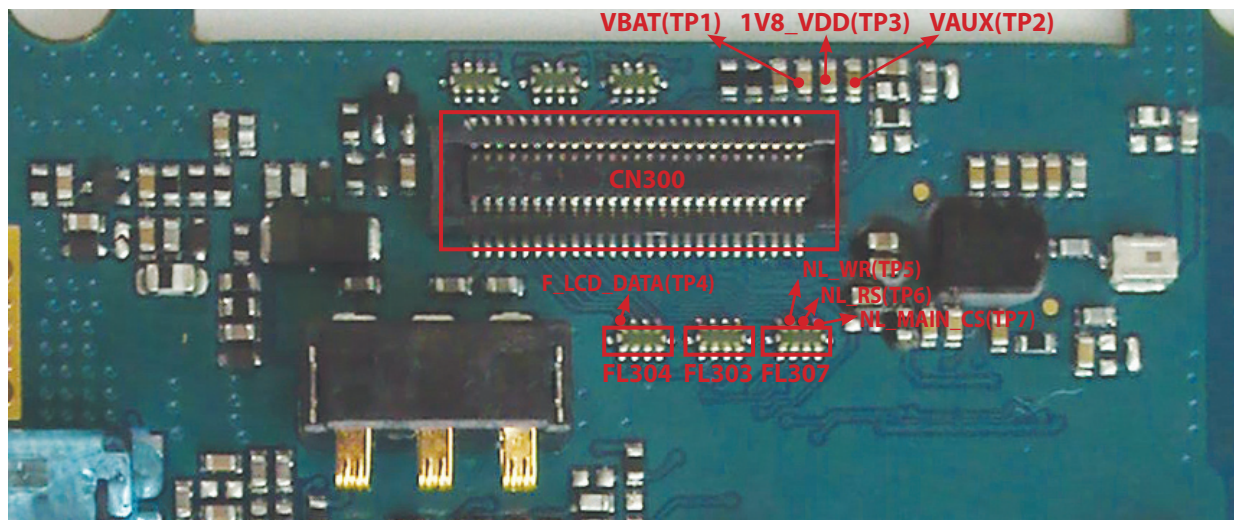


Figure 4.8.1

4. TROUBLE SHOOTING

CIRCUIT

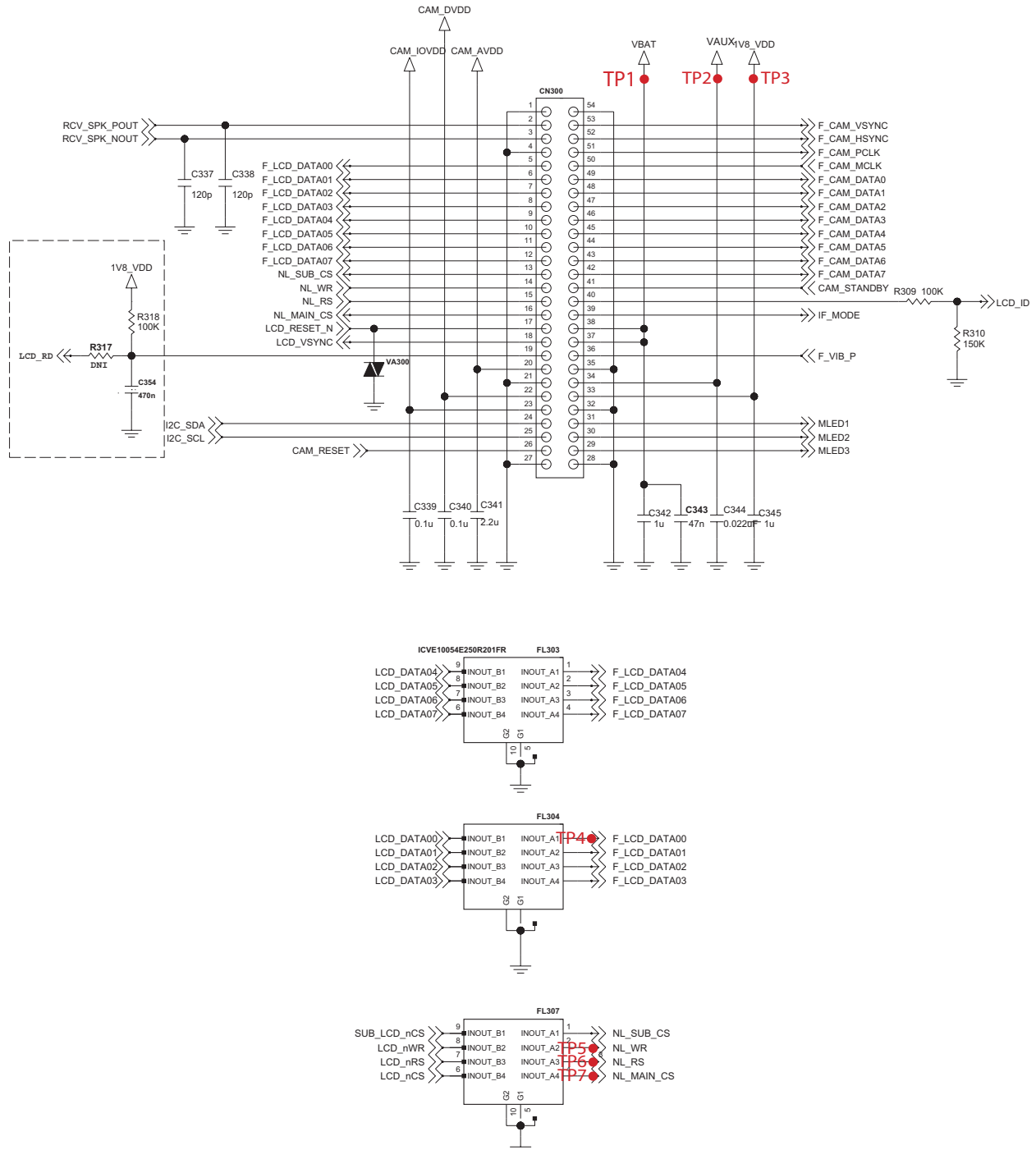
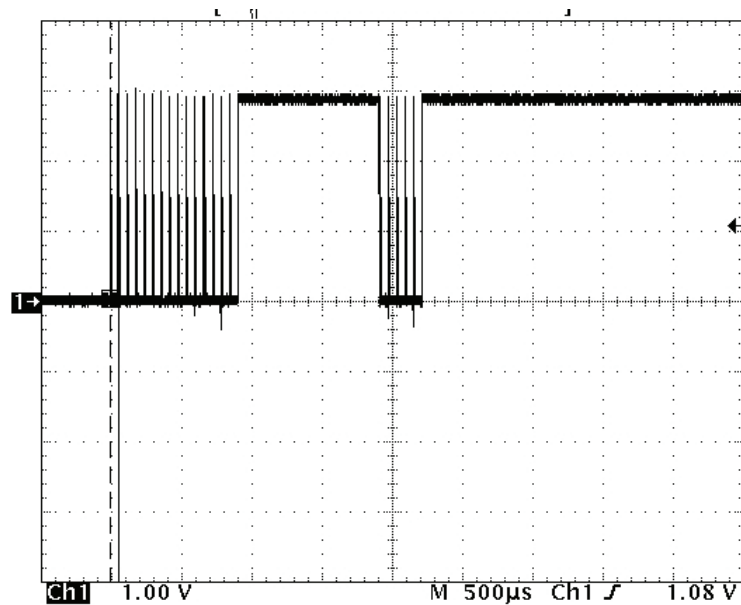
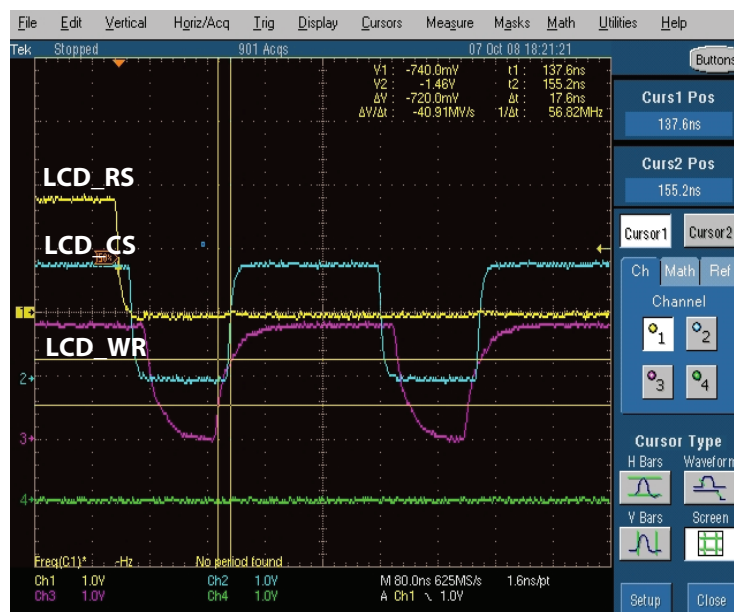


Figure 4.8.2

Waveform

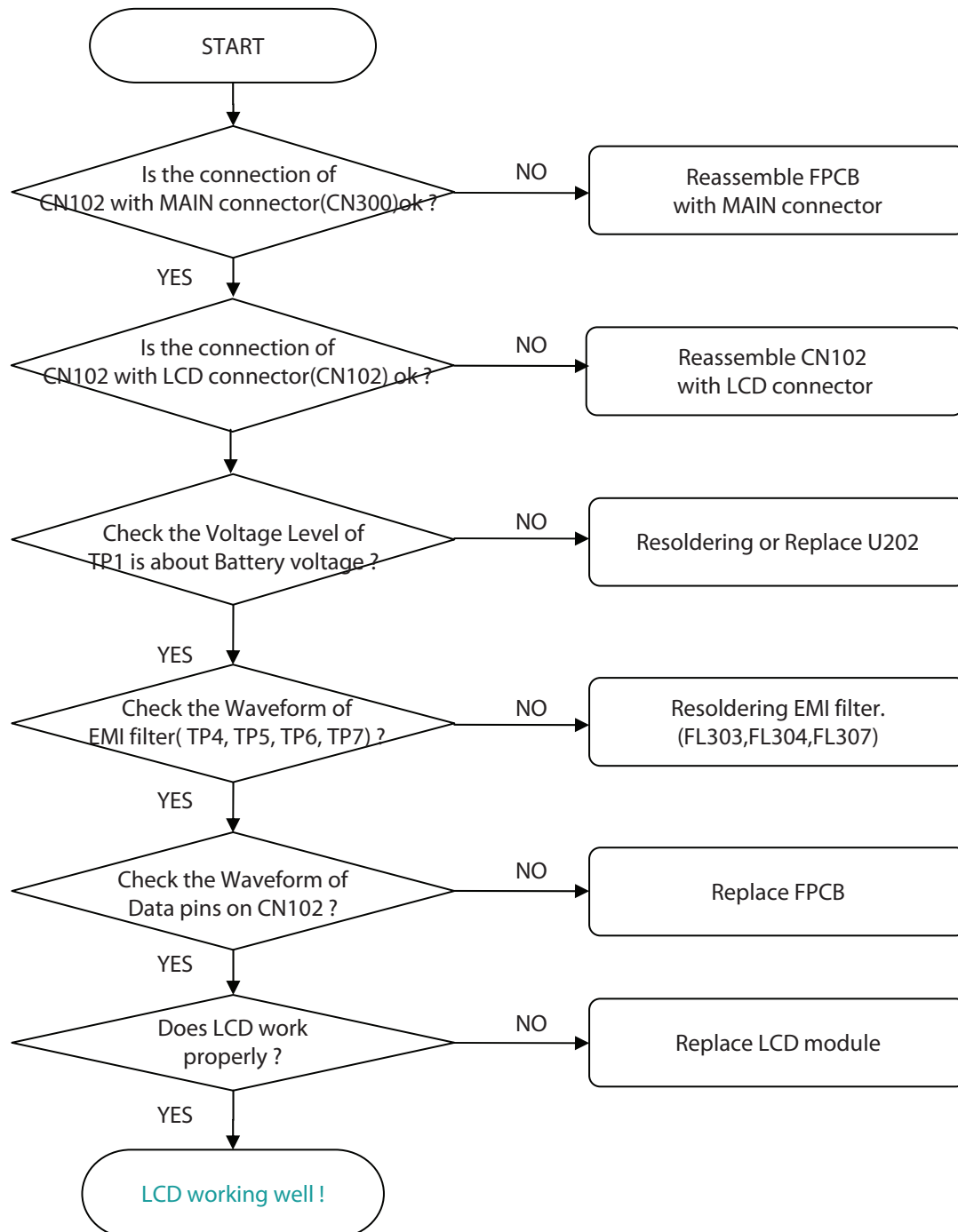


Graph 4.8.1. LCD Backlight Control Signal Waveform



Graph 4.8.2. LCD Data Waveform

CHECKING FLOW



4.9 Camera Trouble

TEST POINT

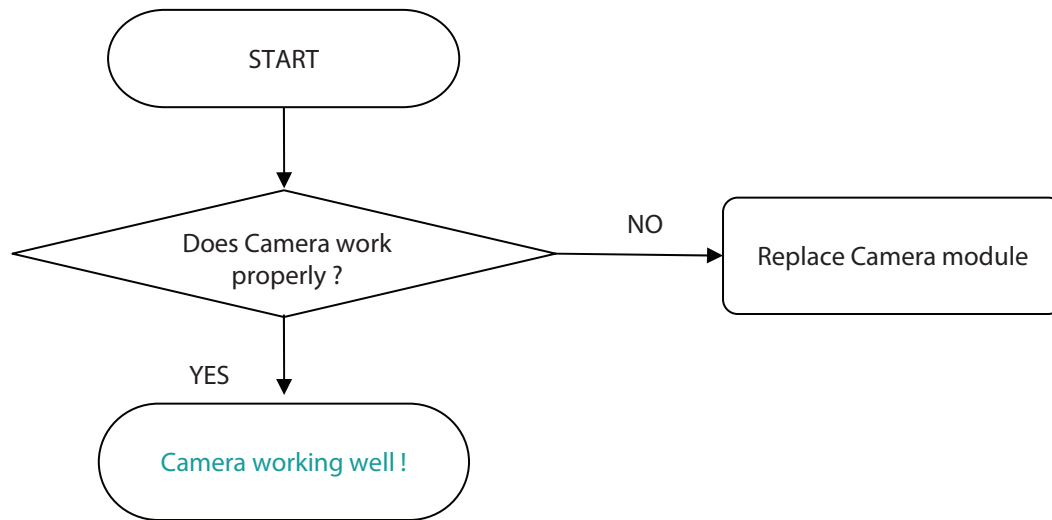


Figure 4.9.1

CIRCUIT



CHECKING FLOW



4.10 Speaker Trouble

TEST POINT

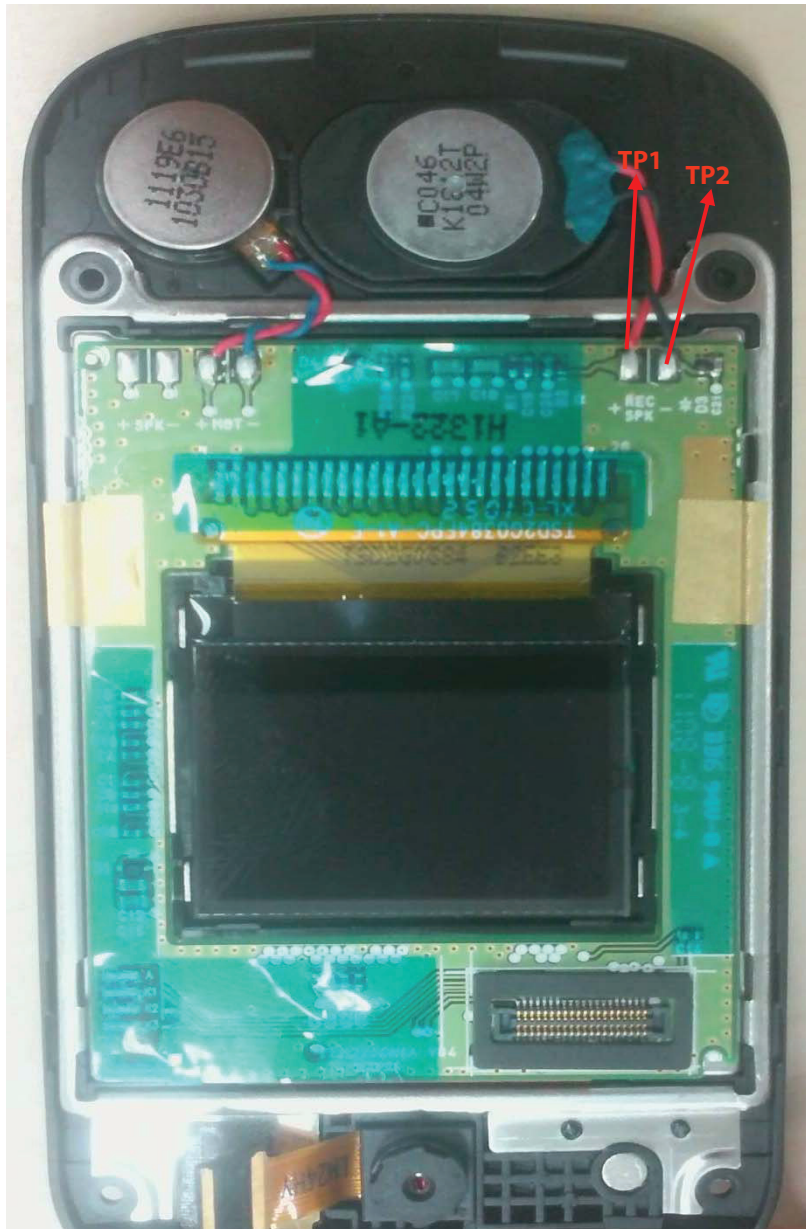


Figure 4.10.1

CIRCUIT

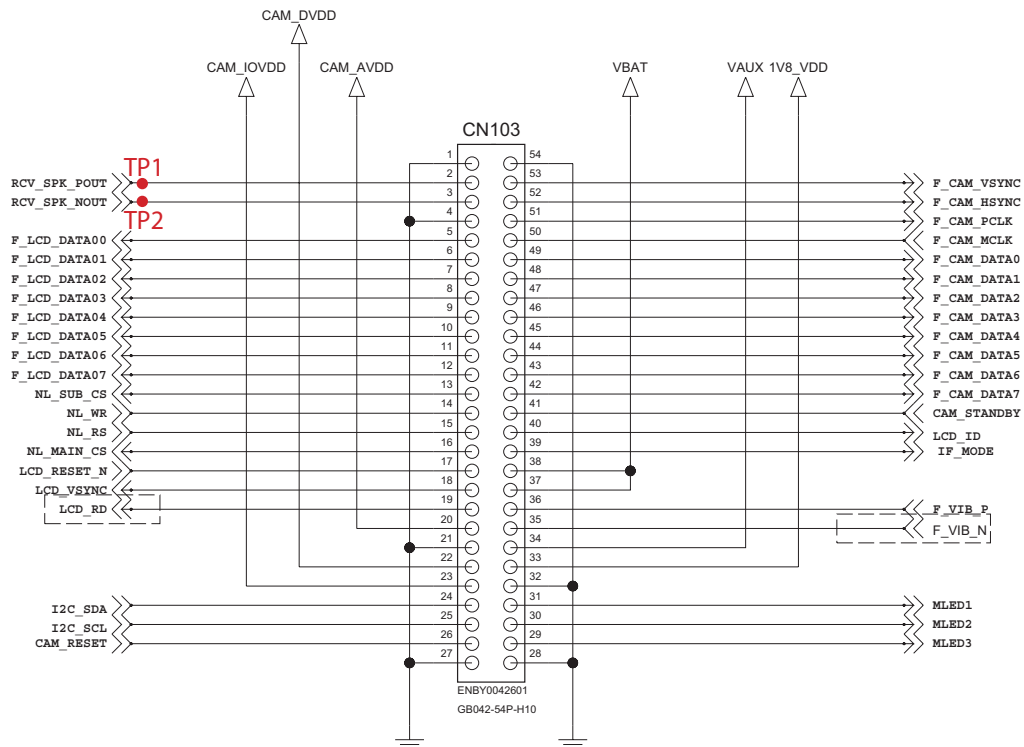
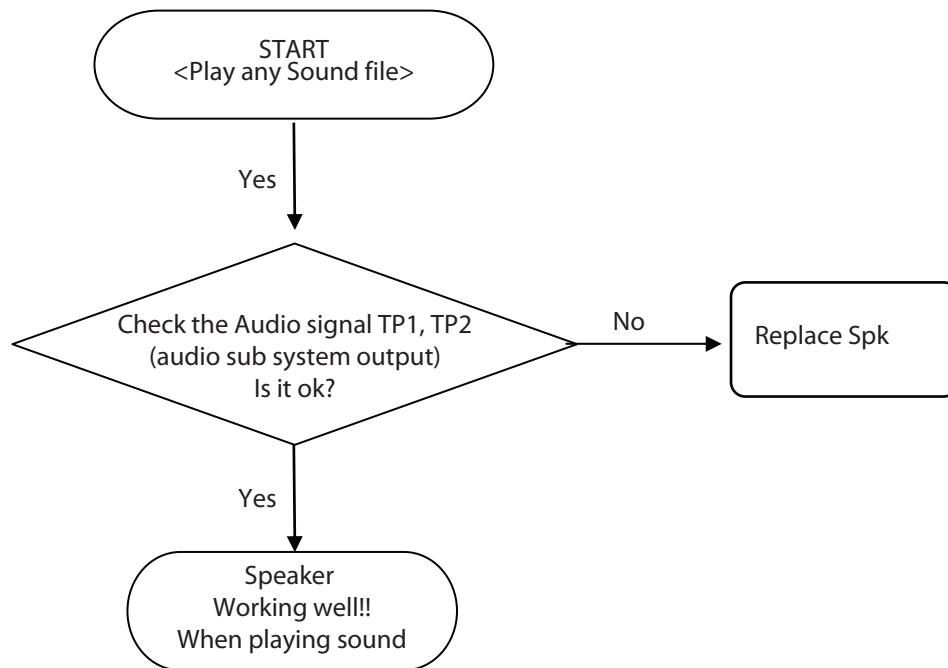


Figure 4.10.3

CHECKING FLOW



4.11 Earphone Trouble

TEST POINT

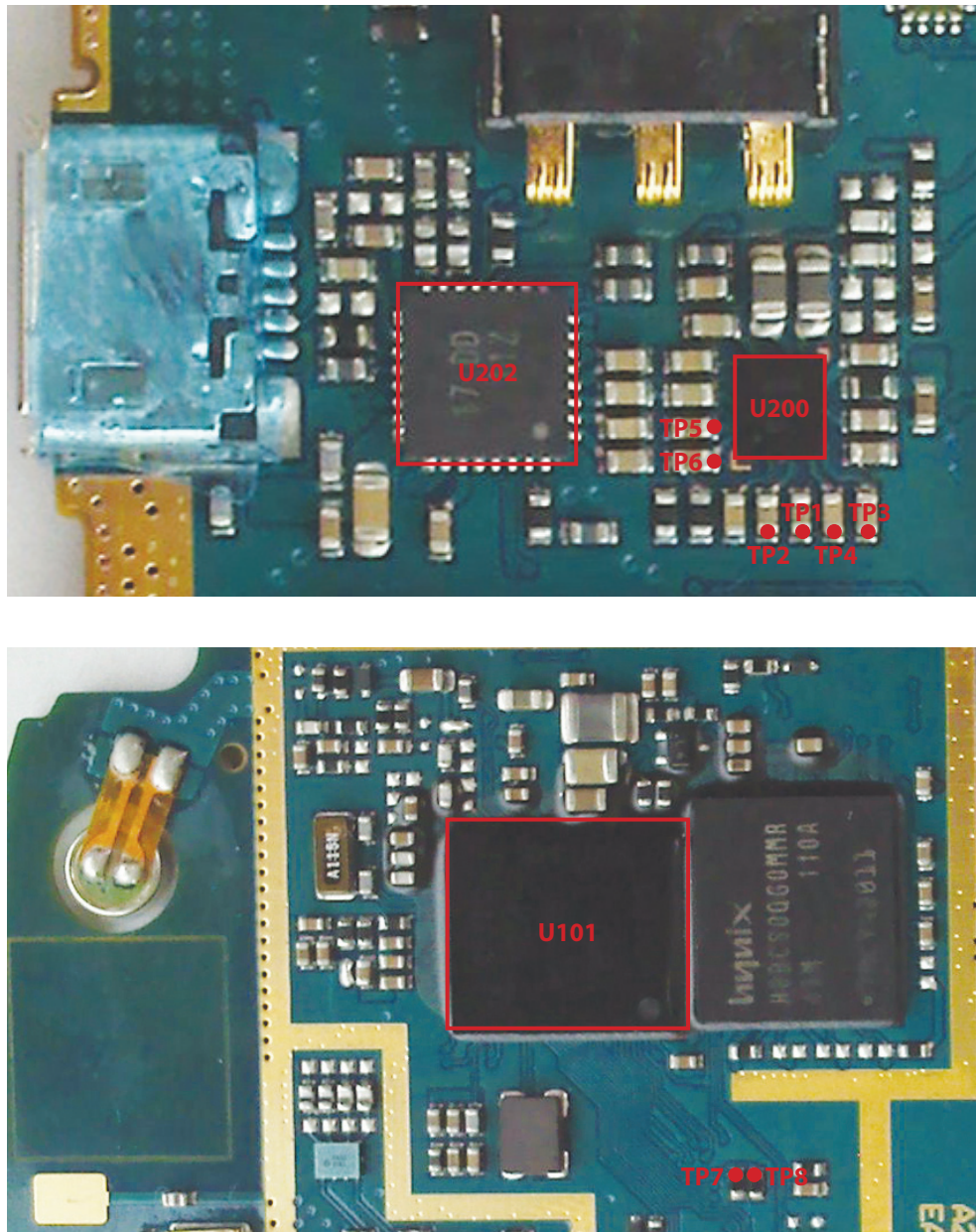
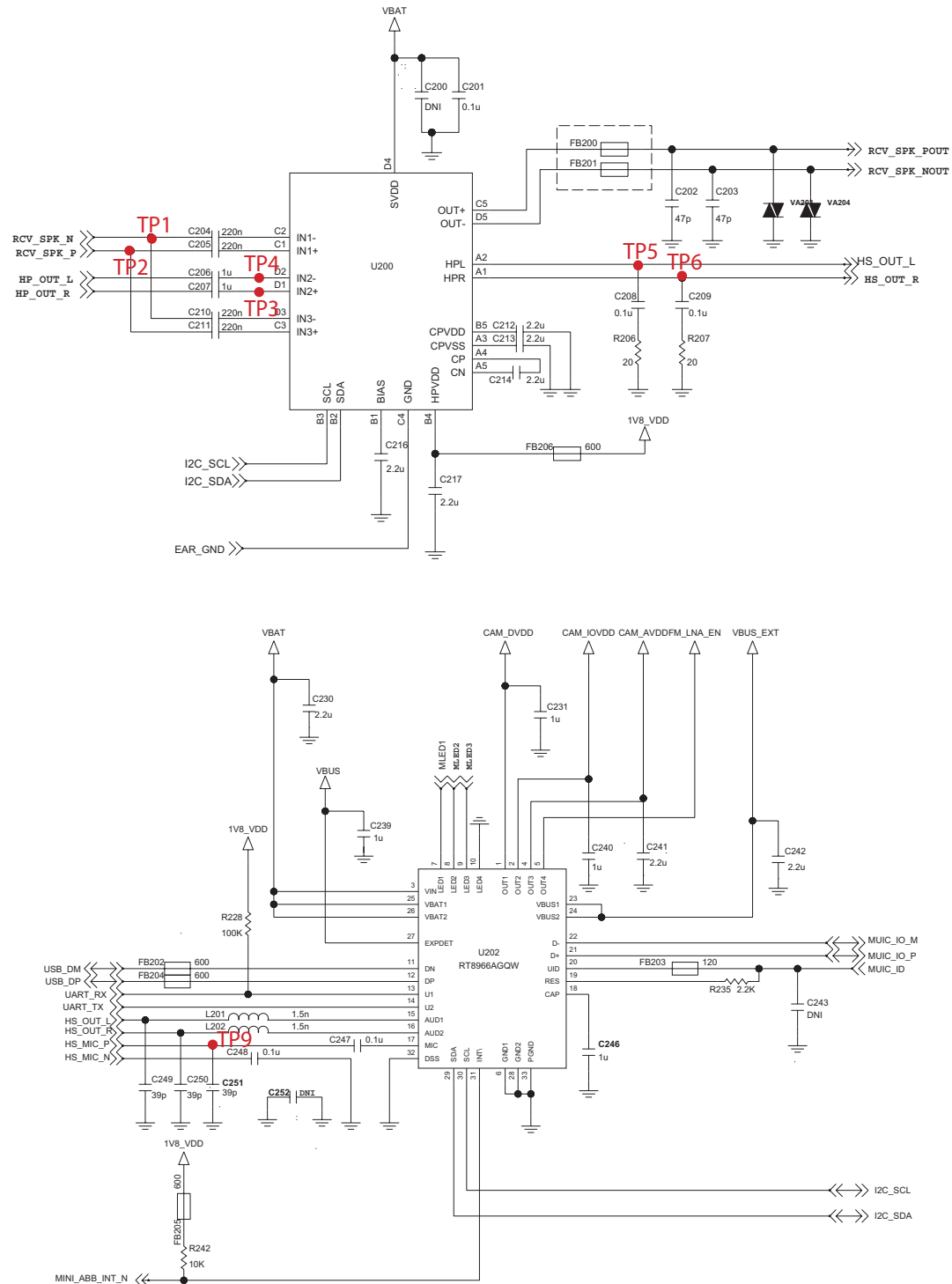


Figure 4.11.1

4. TROUBLE SHOOTING

CIRCUIT



CIRCUIT

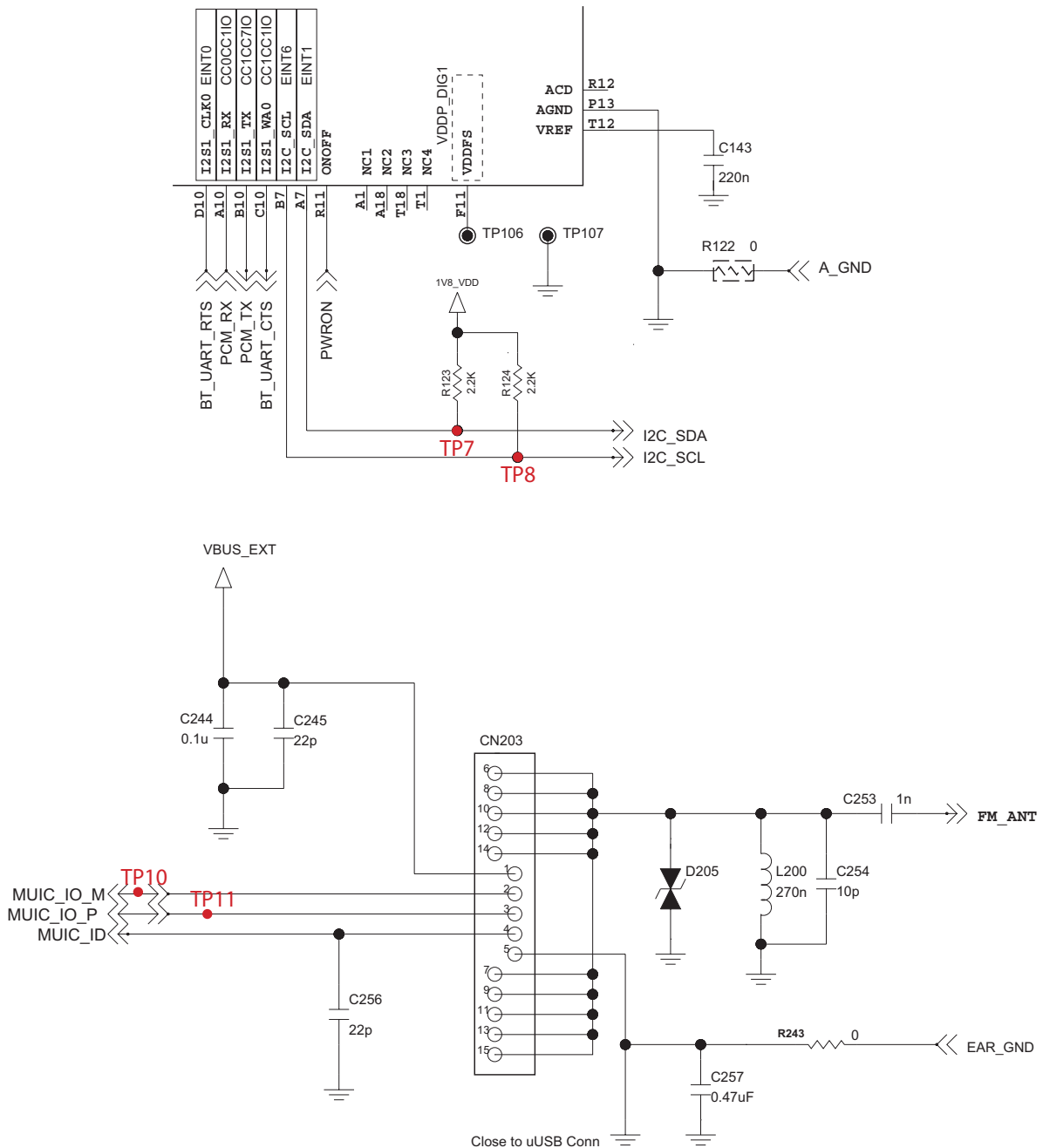
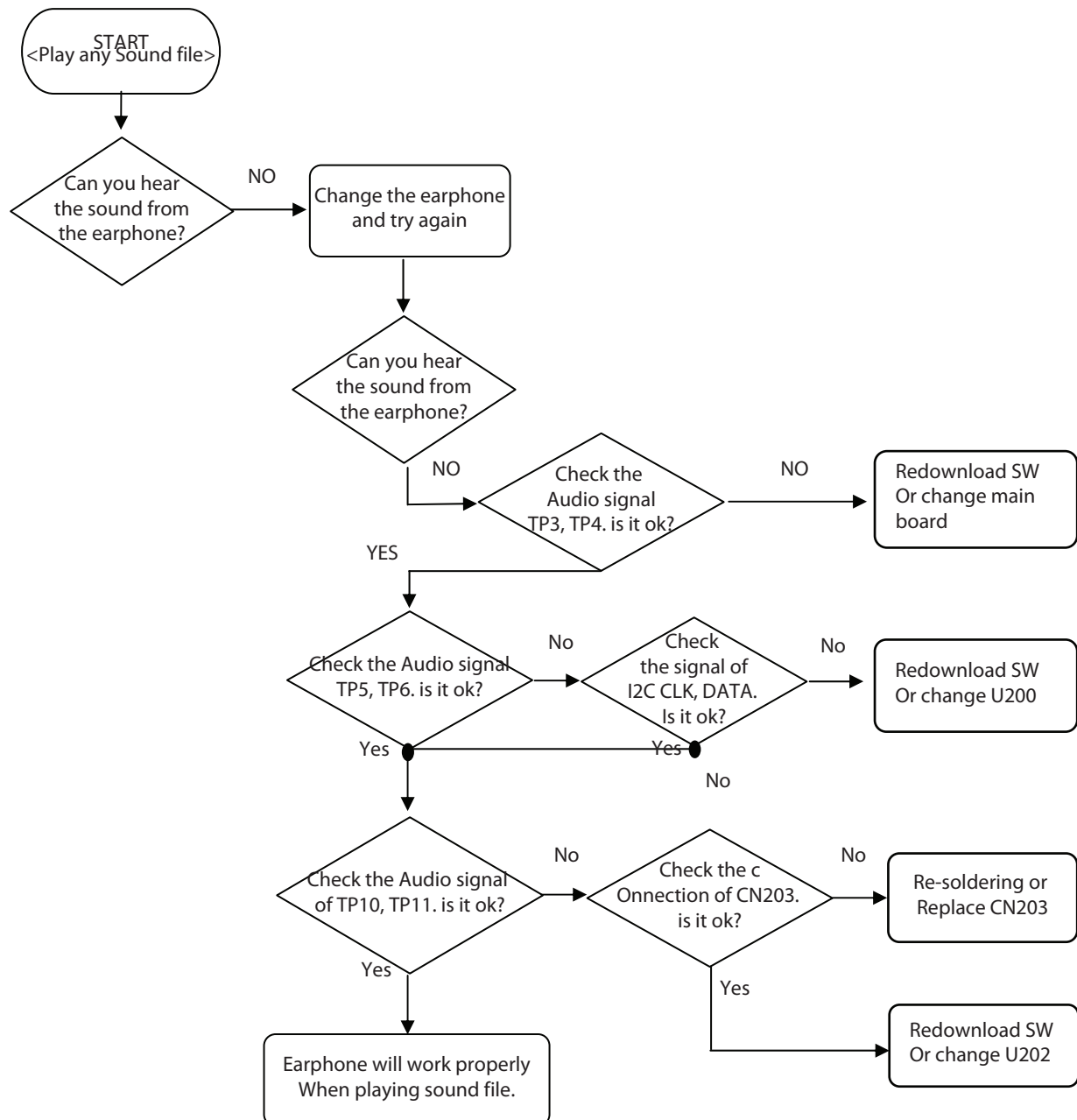
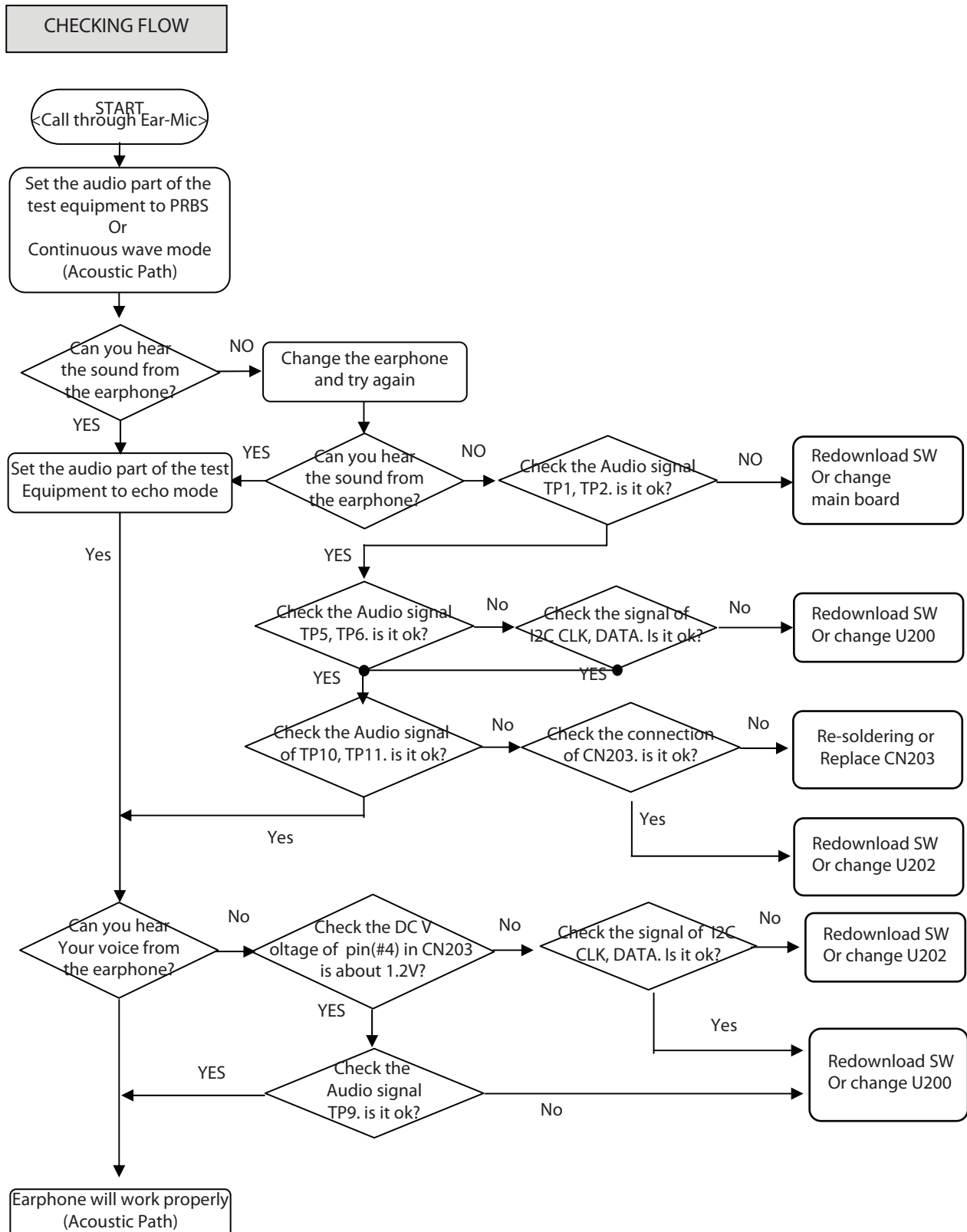


Figure 4.11.3

CHECKING FLOW





4.12 Micro SD Trouble

TEST POINT

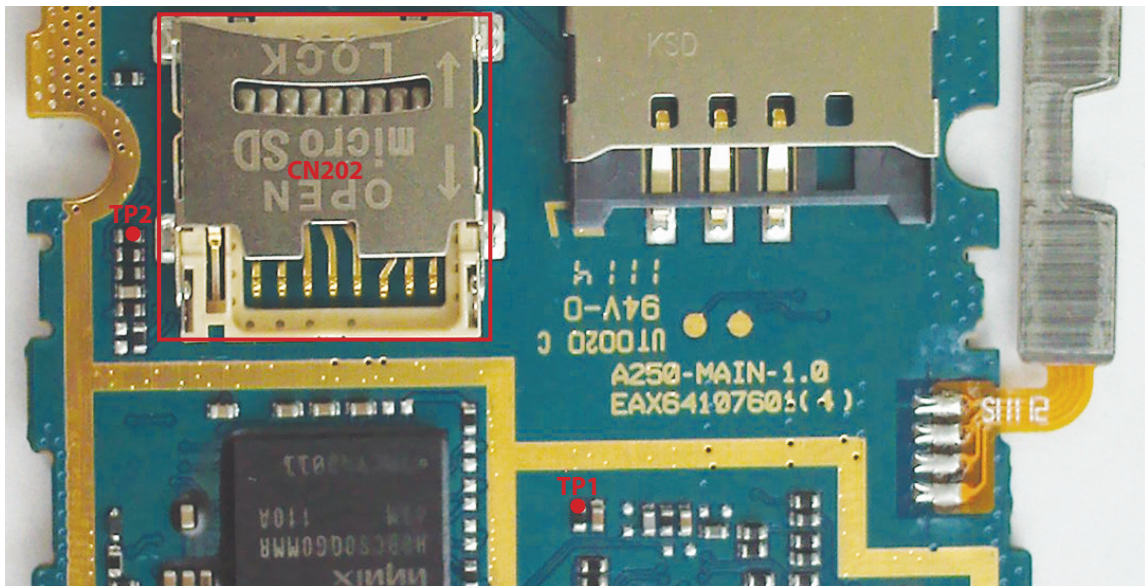


Figure 4.12.1

CIRCUIT

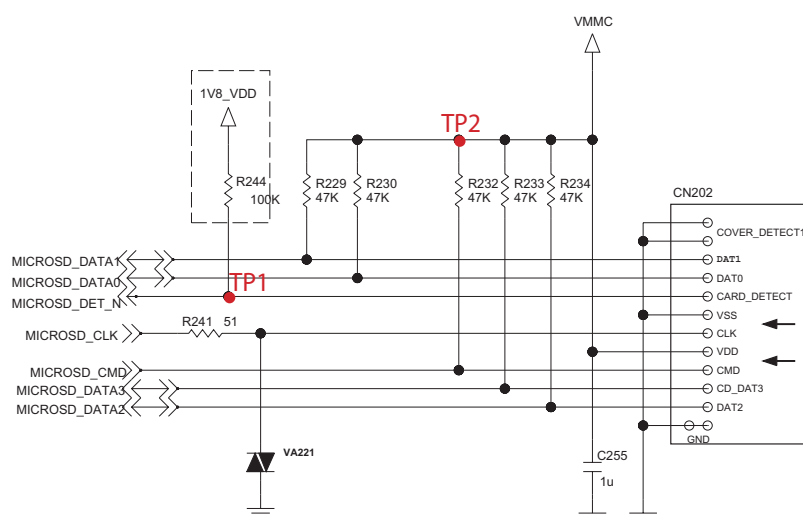
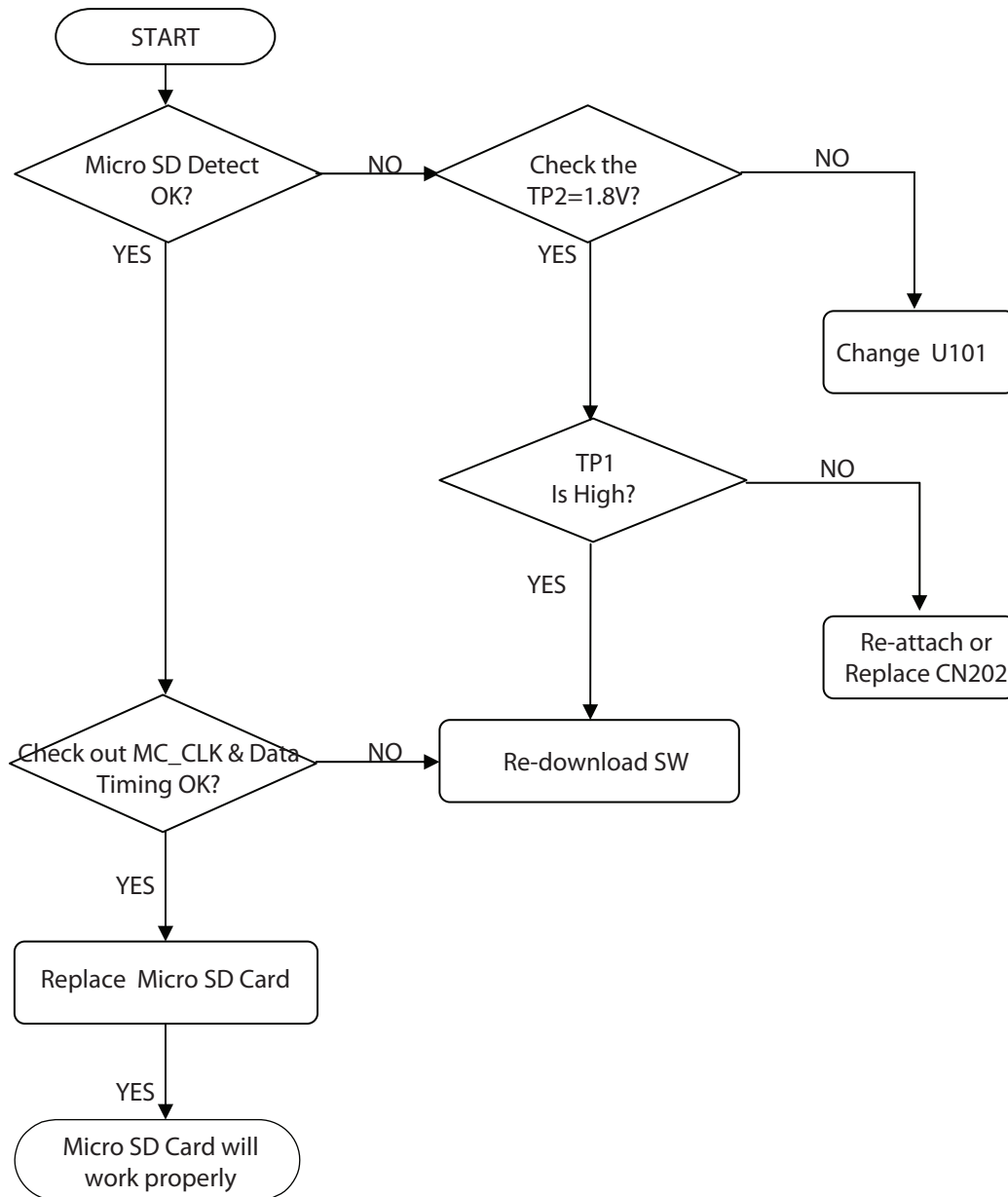


Figure 4.12.2

CHECKING FLOW



4.13 Bluetooth Trouble

TEST POINT

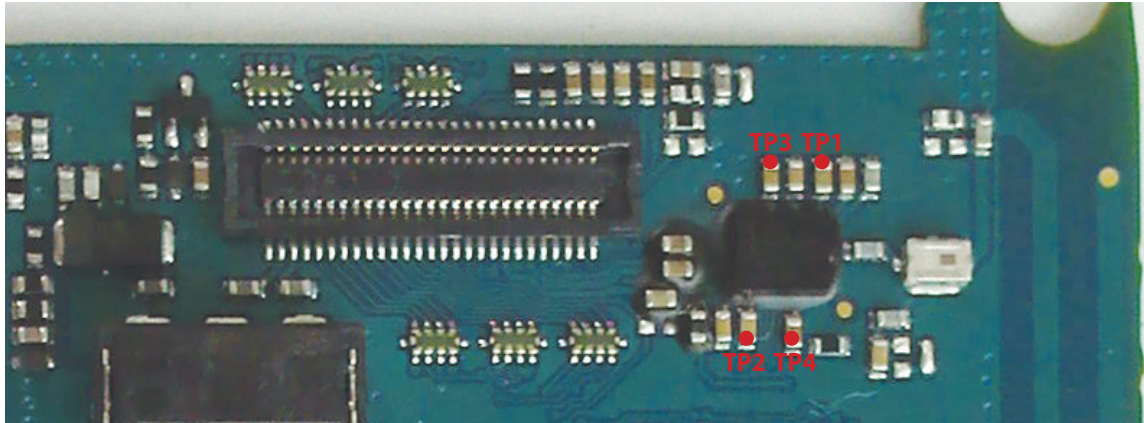


Figure 4.13.1 Bluetooth block

CIRCUIT

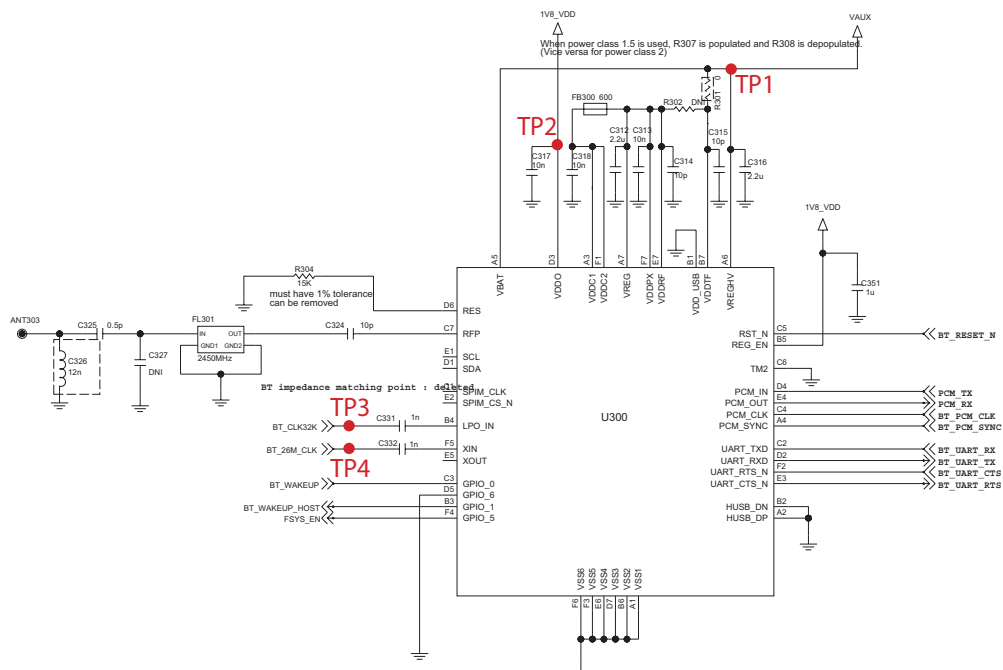
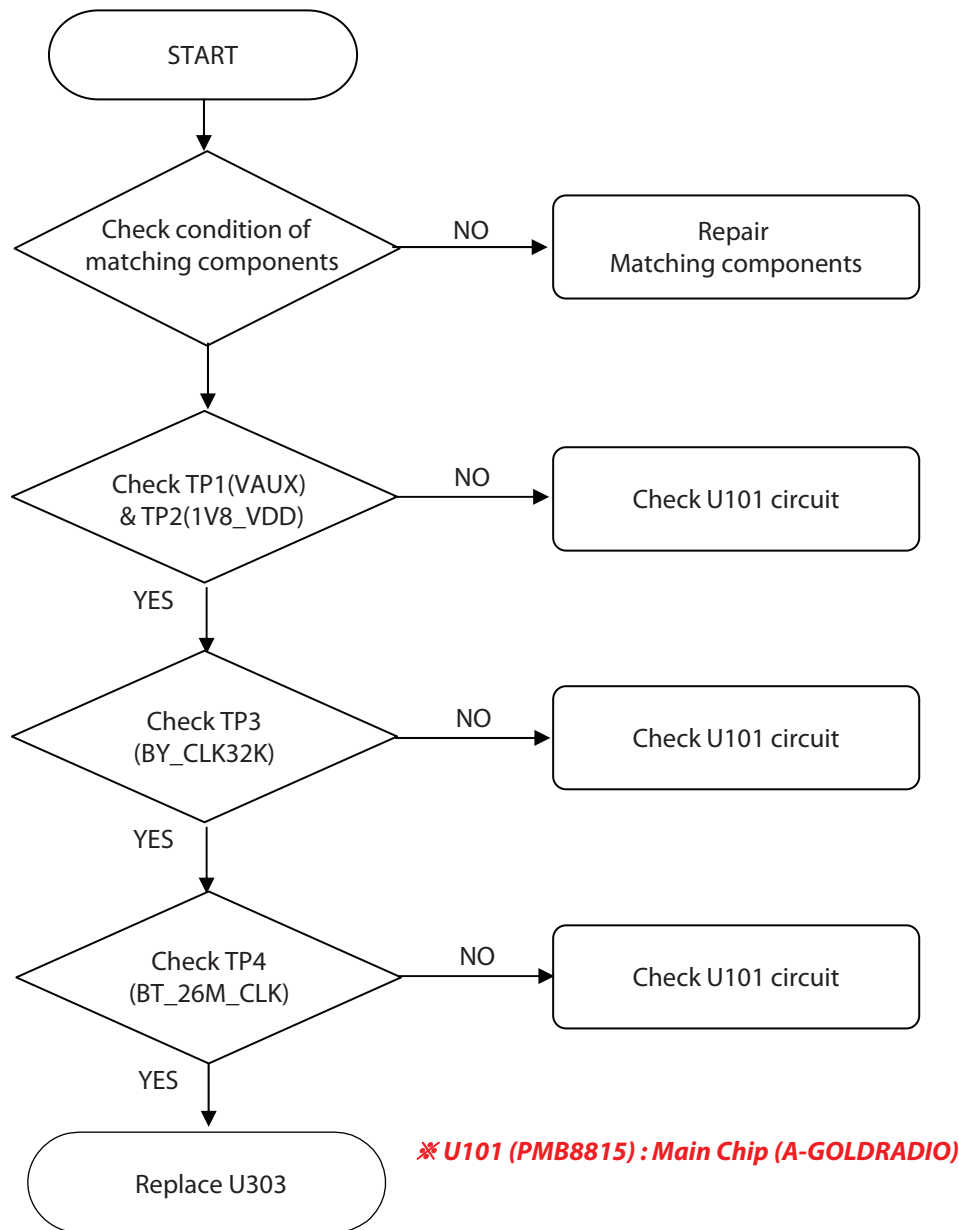


Figure 4.13.2 Bluetooth circuit

CHECKING FLOW



4.14 FM Radio Trouble

TEST POINT

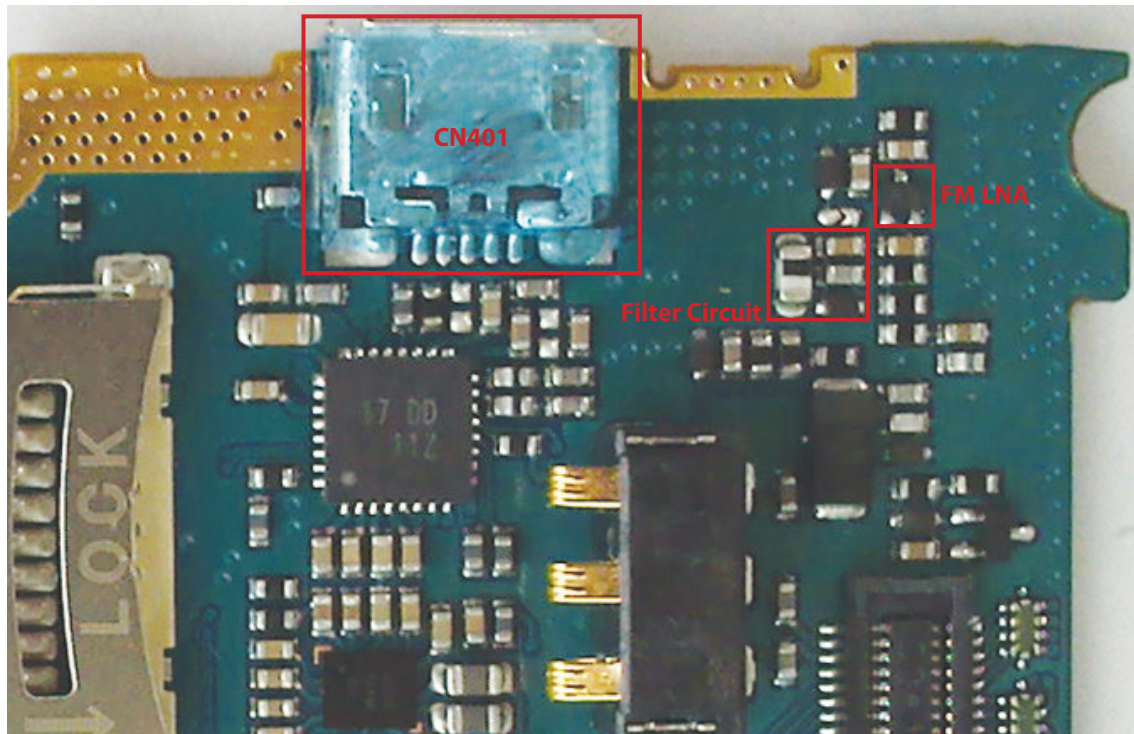


Figure 4.14.1 FM Radio test point

CIRCUIT

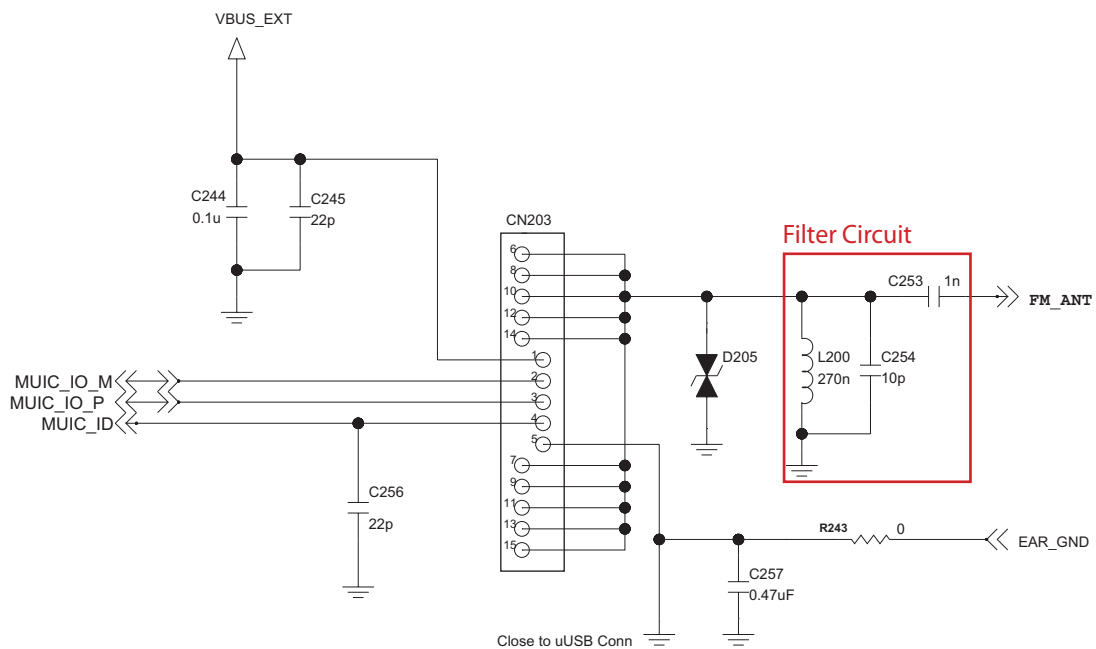
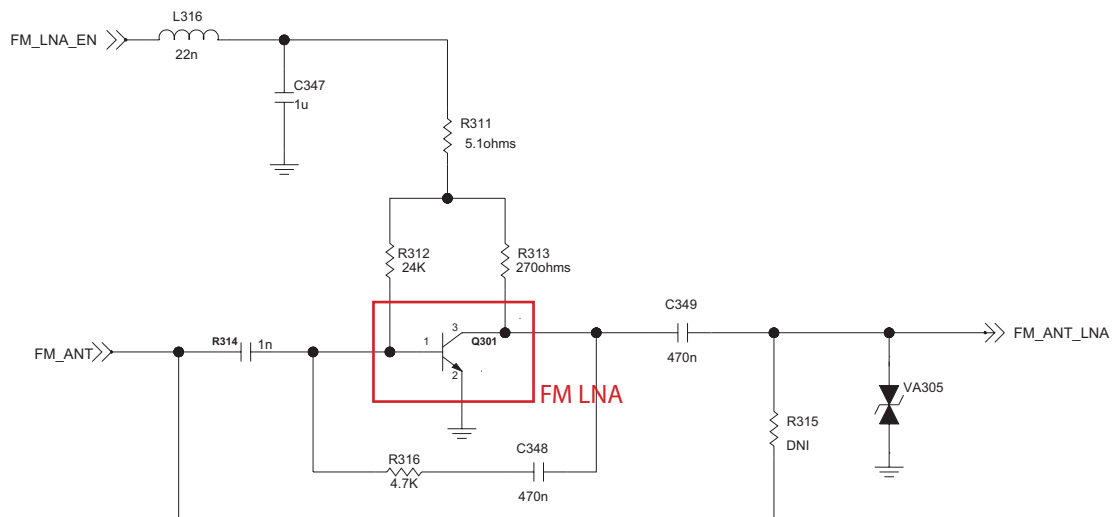
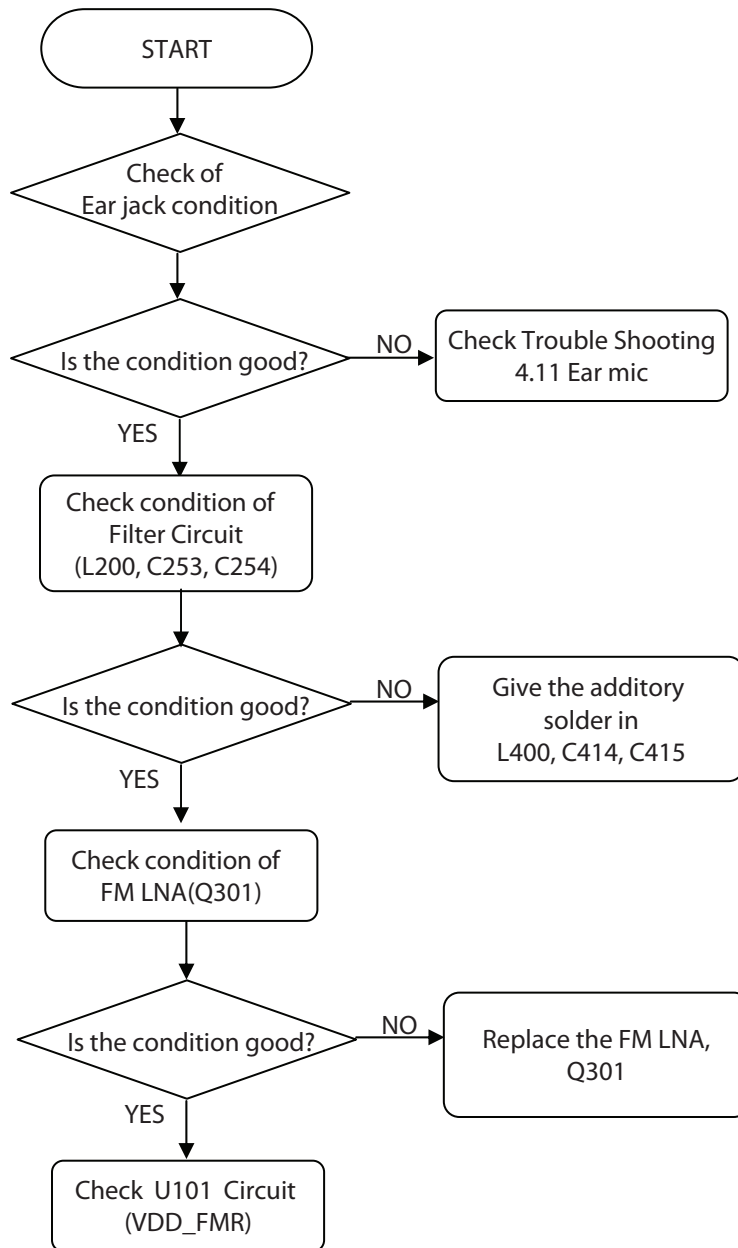
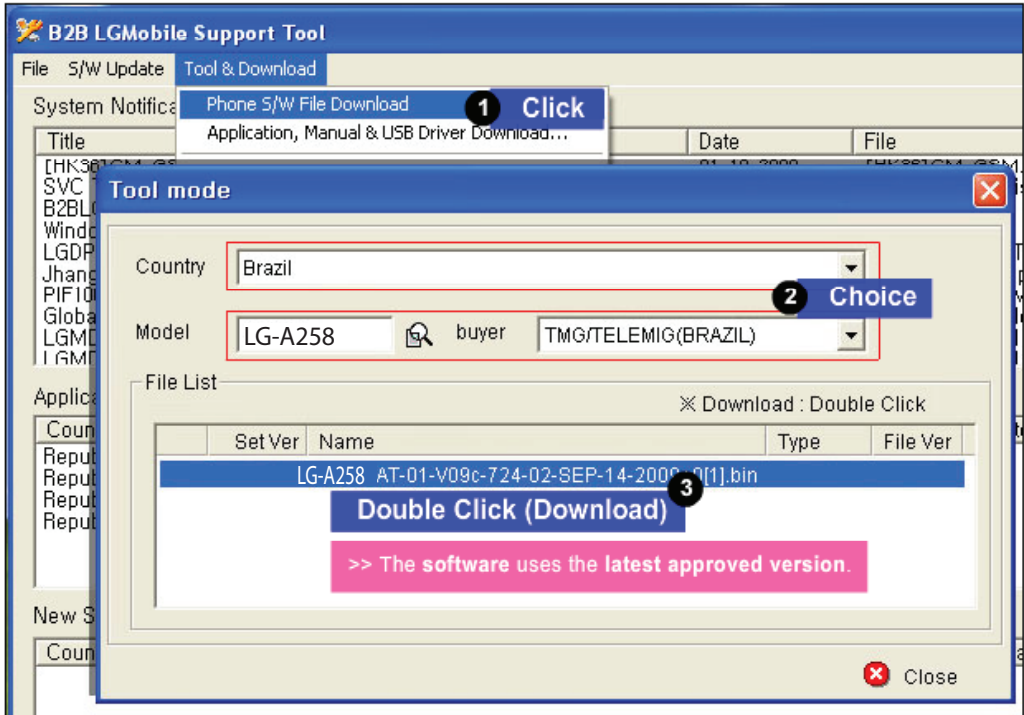
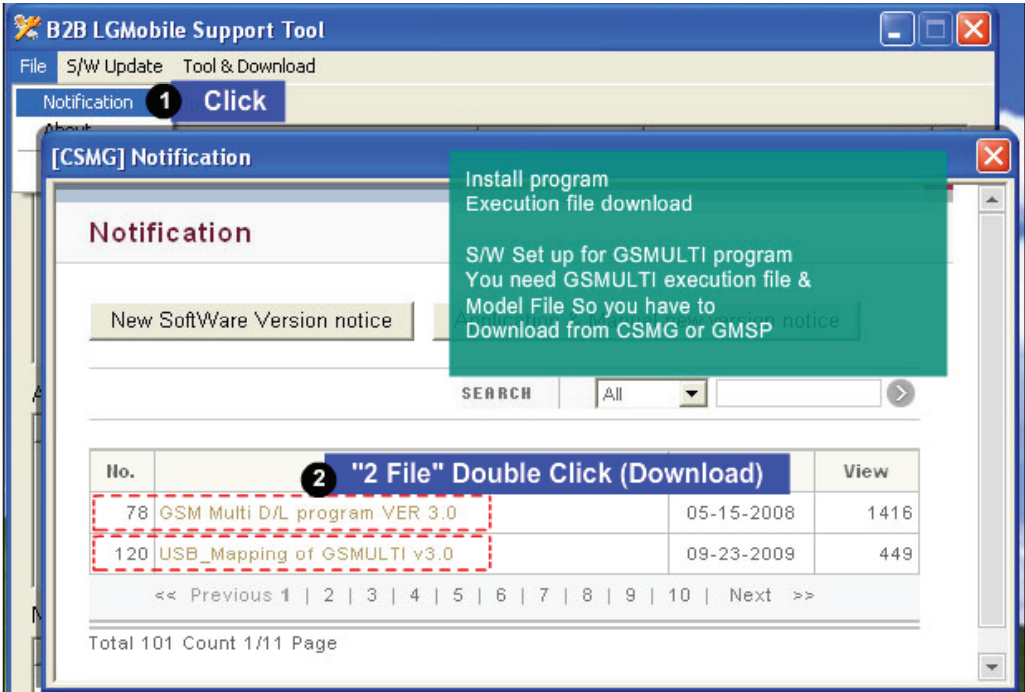


Figure 4.18.2

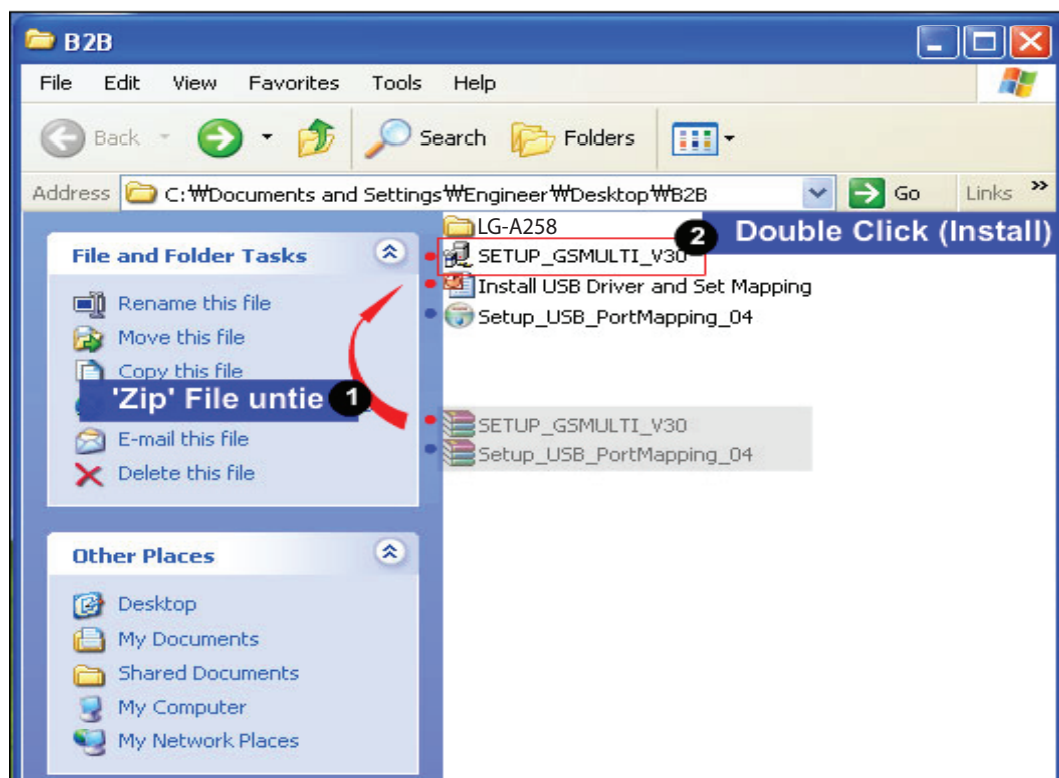
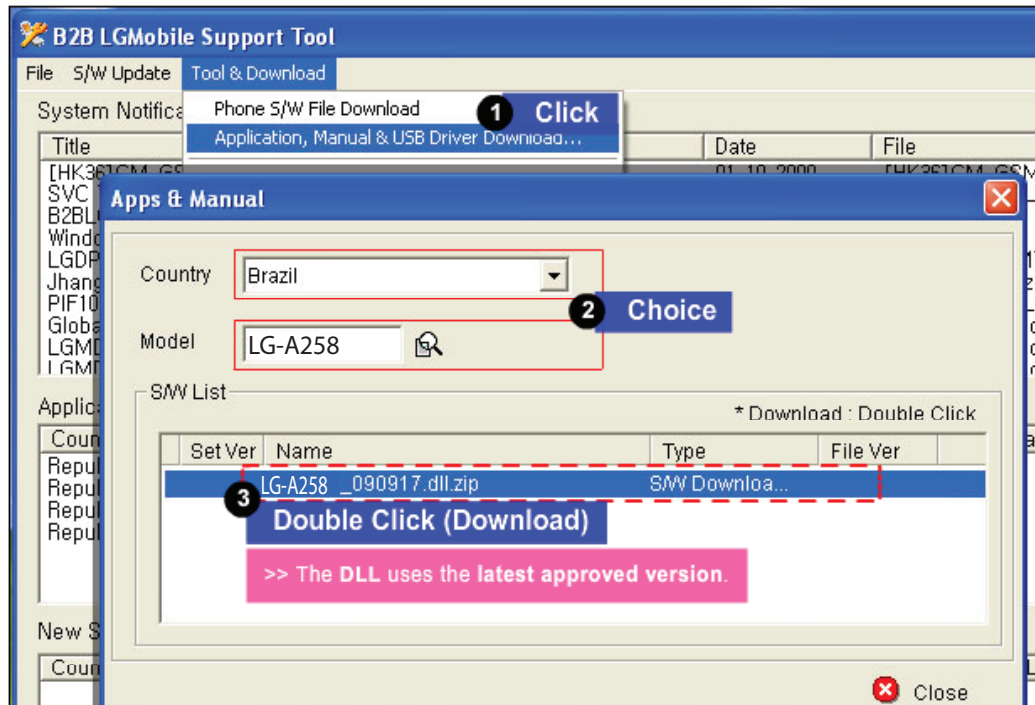
CHECKING FLOW



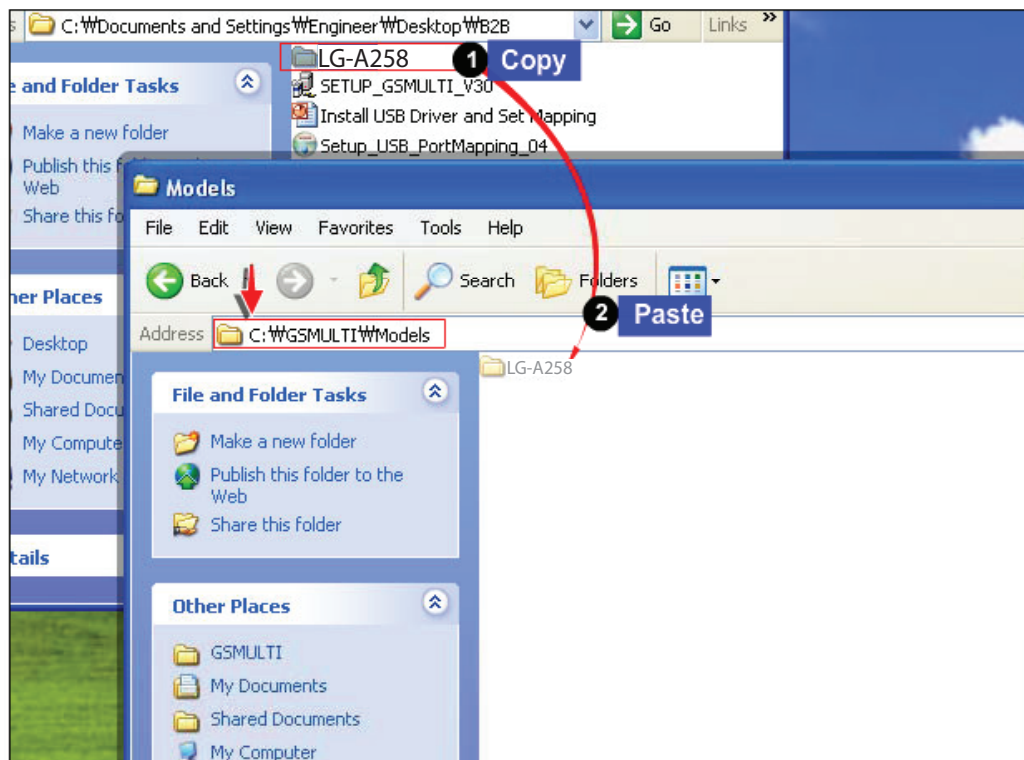
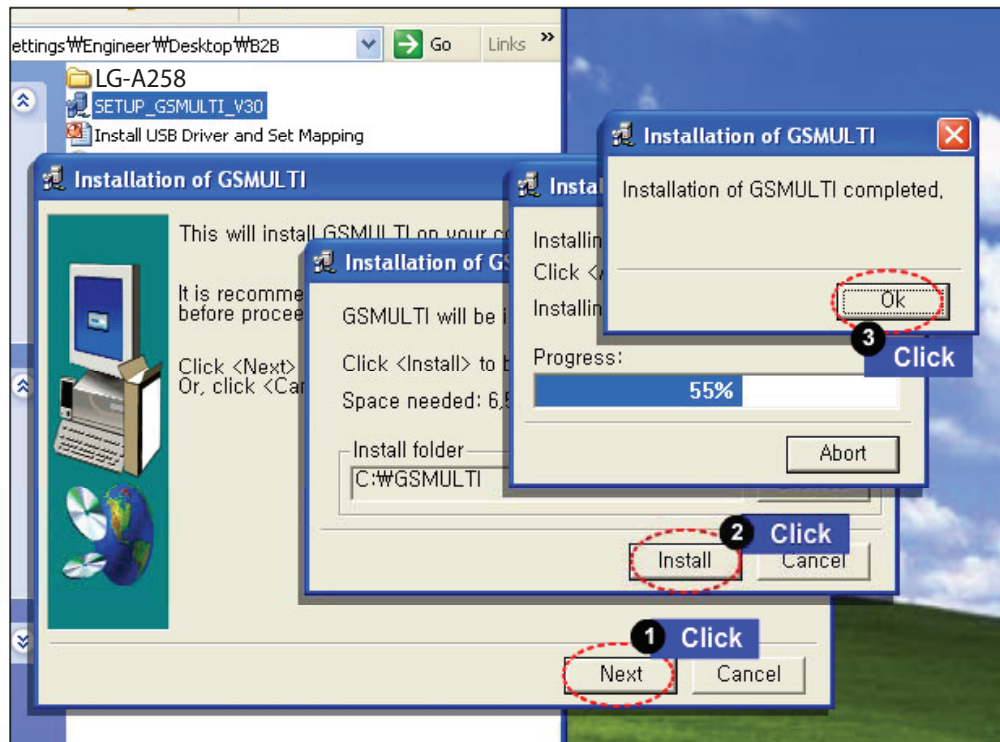
5. DOWNLOAD



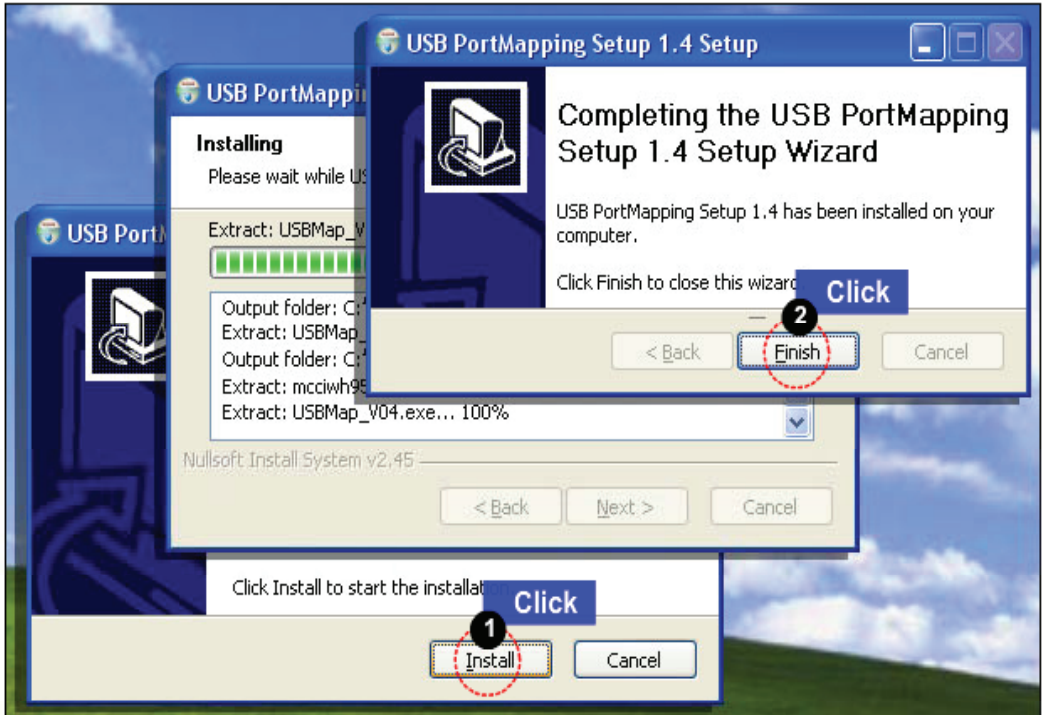
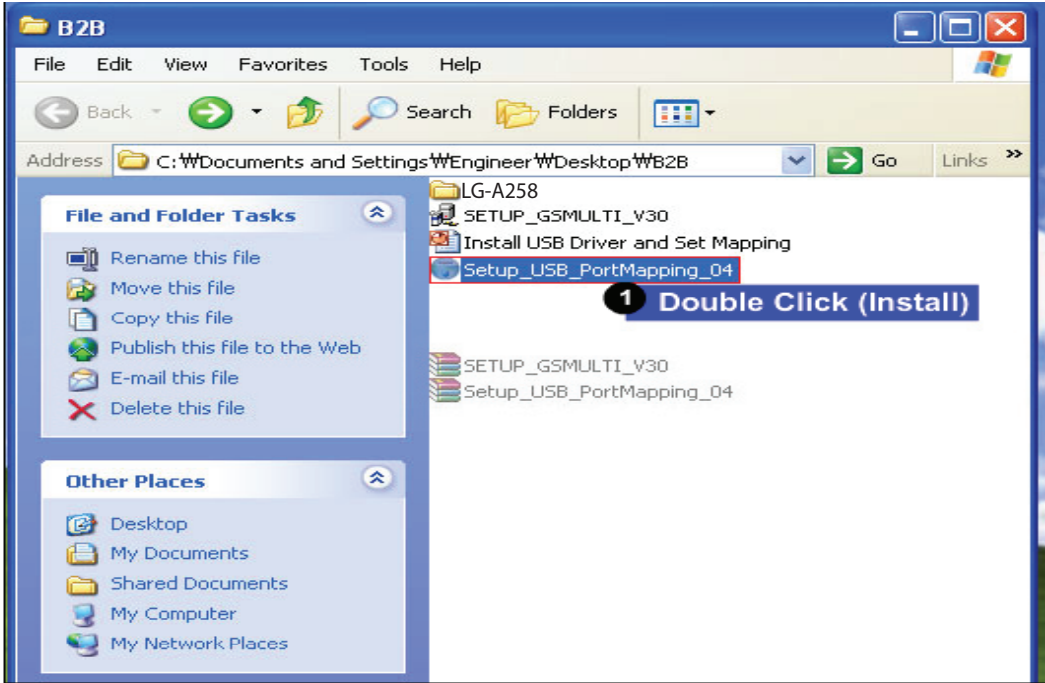
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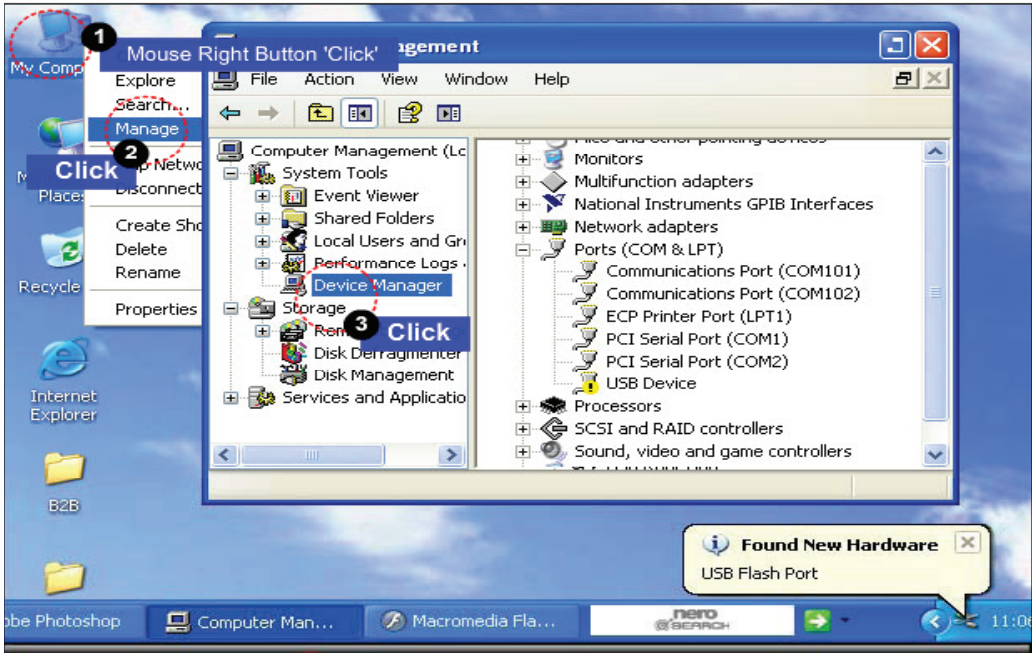
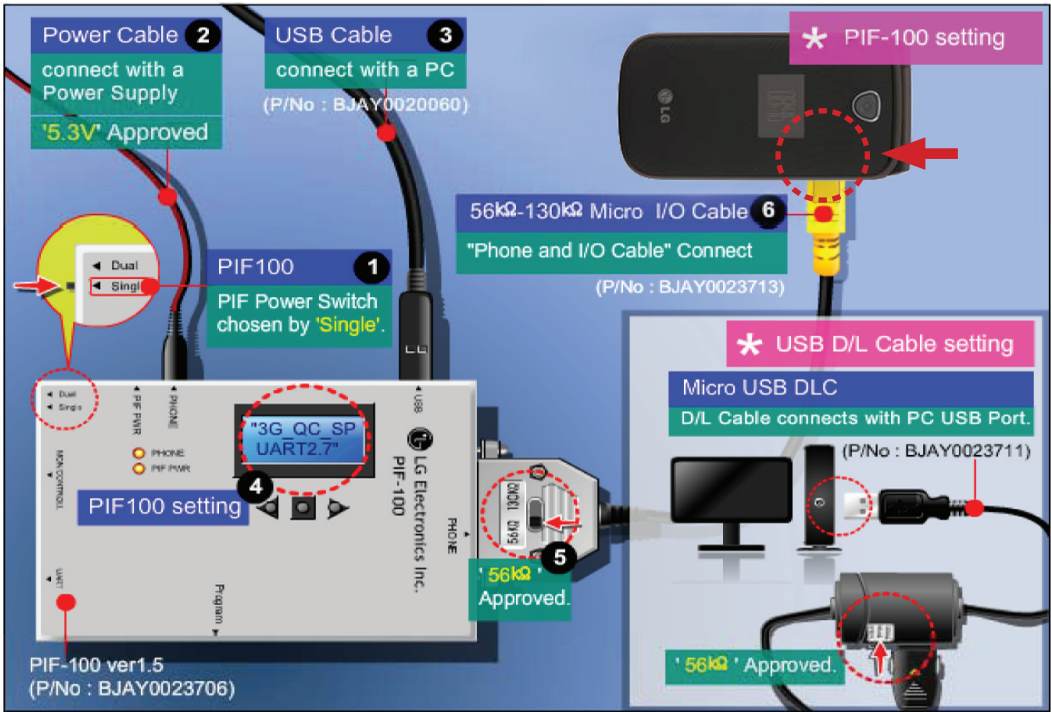


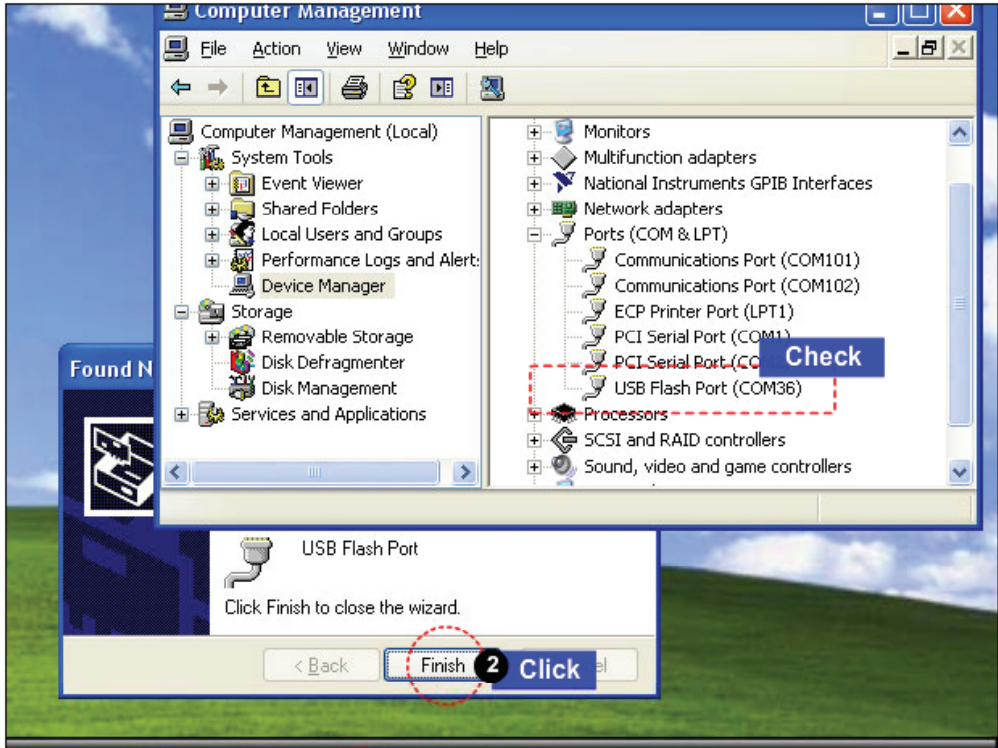
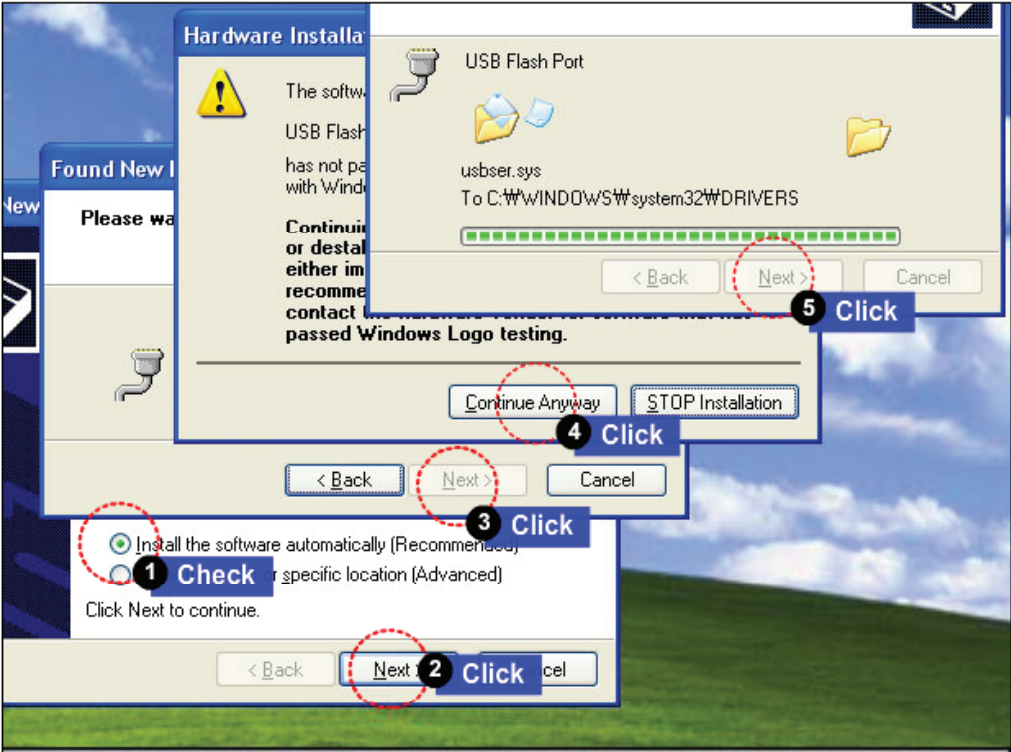
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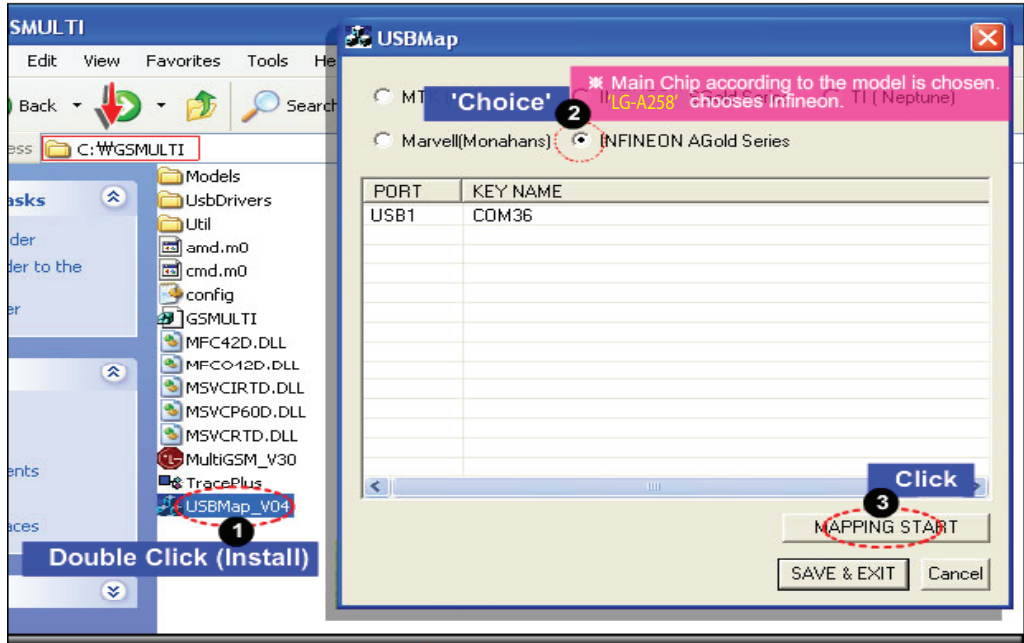


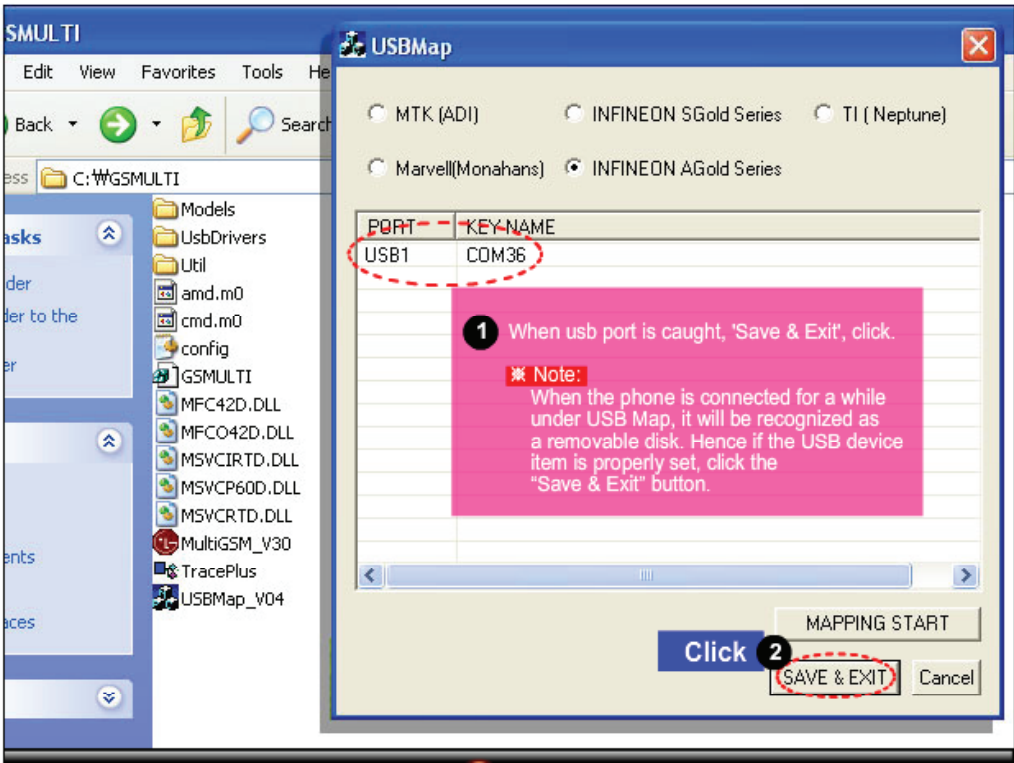
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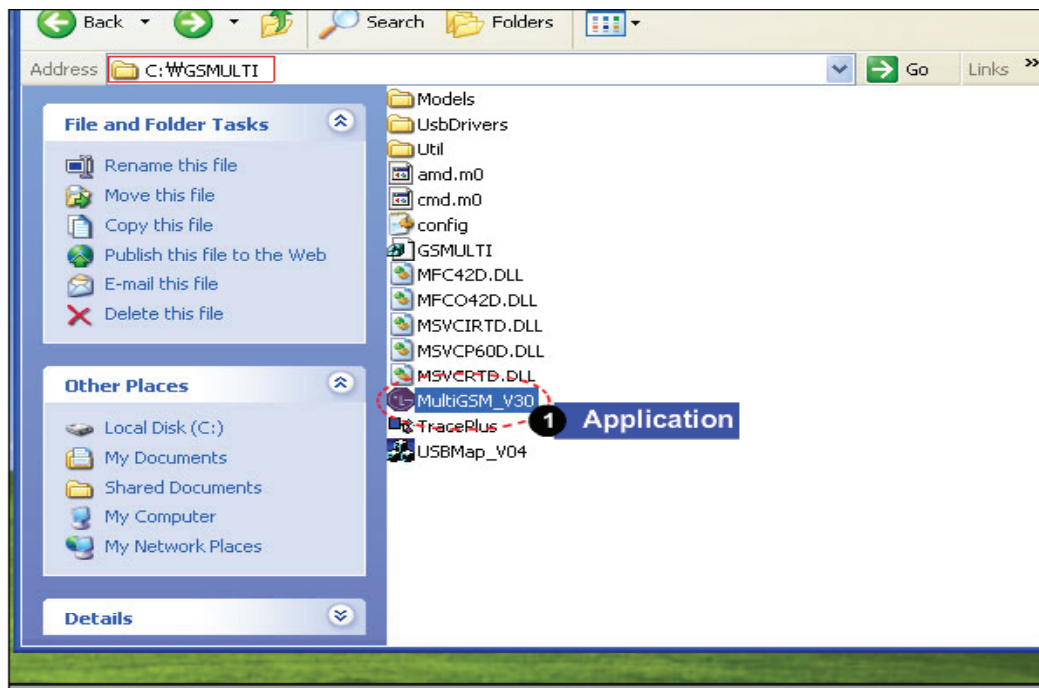
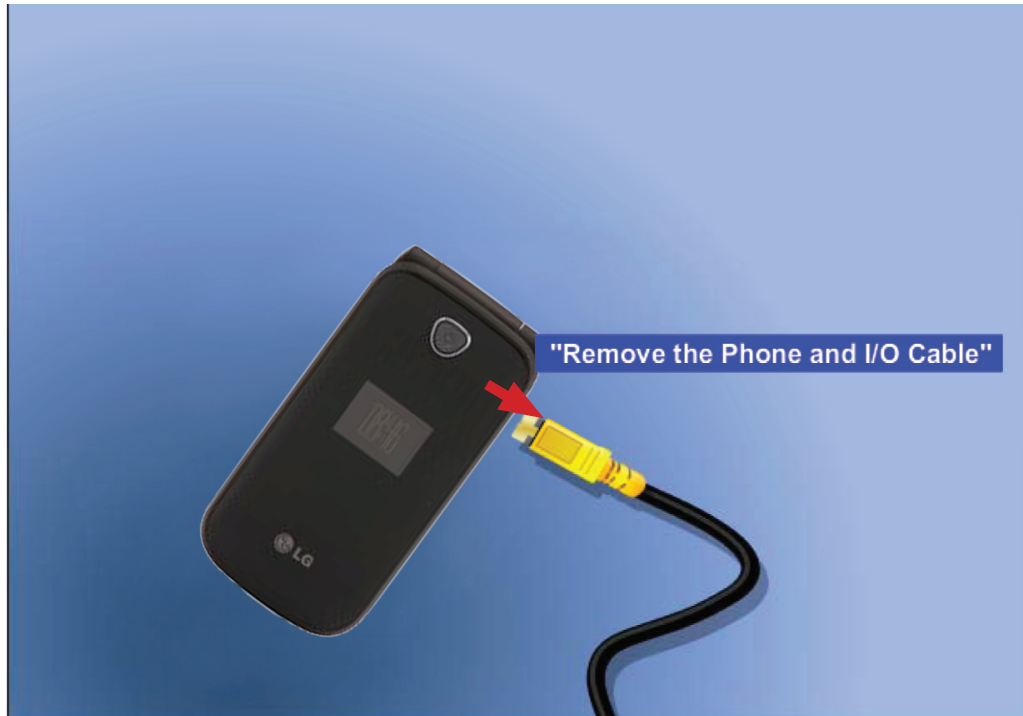




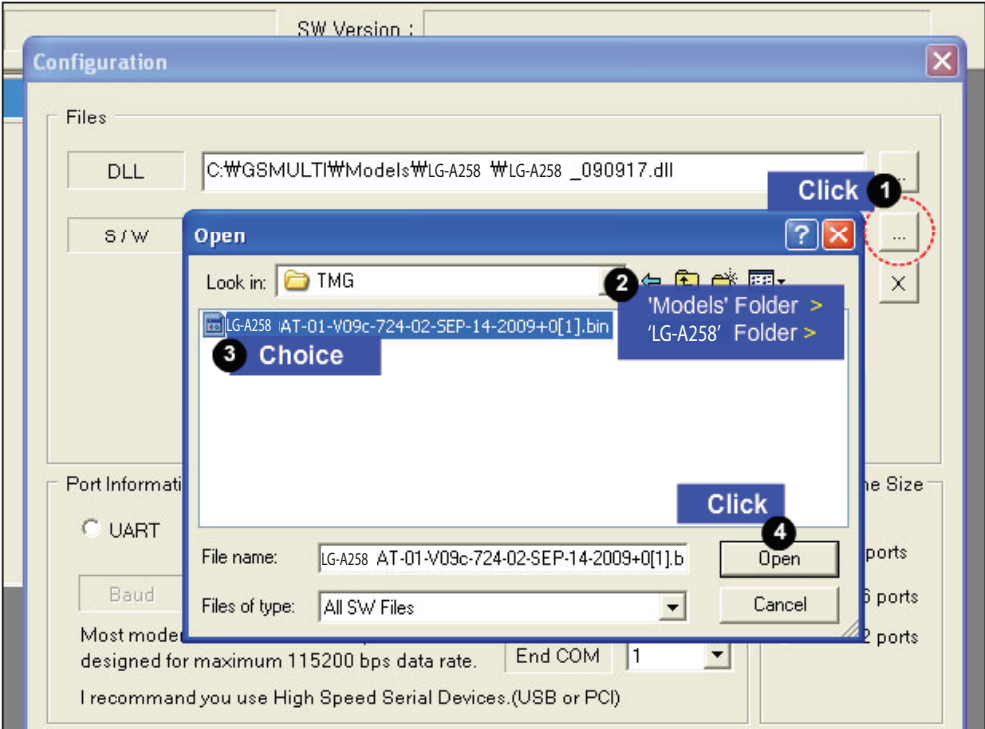
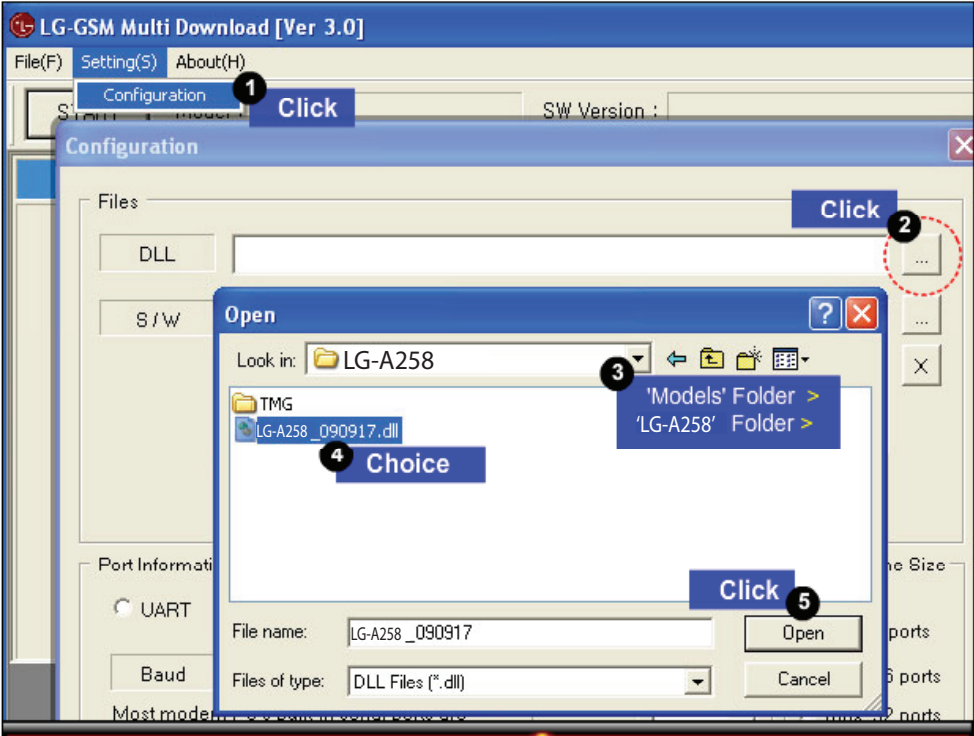




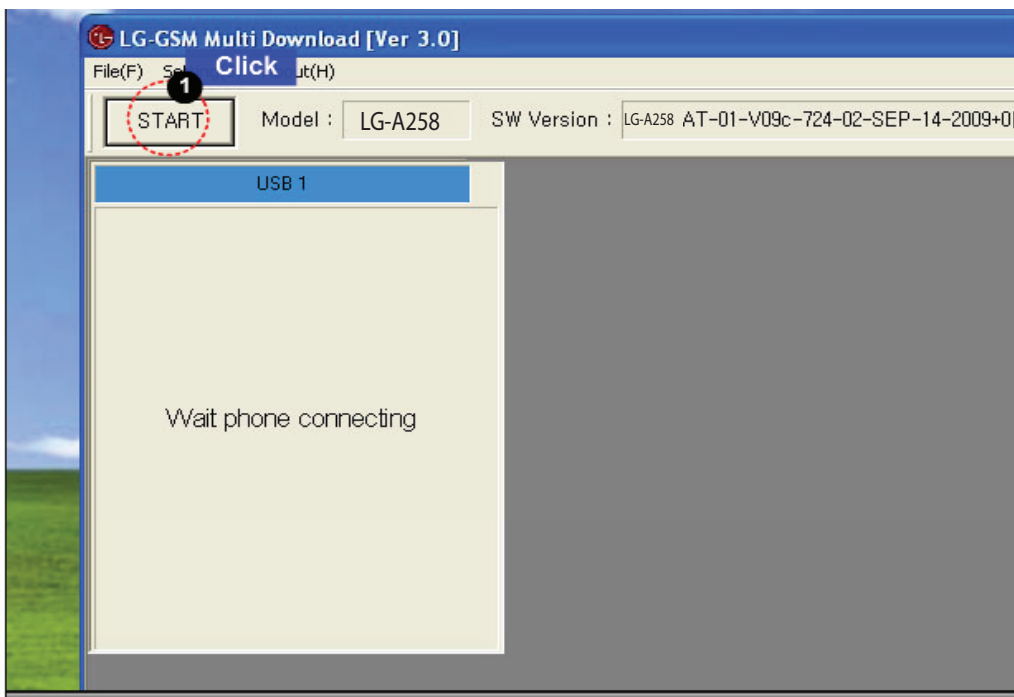
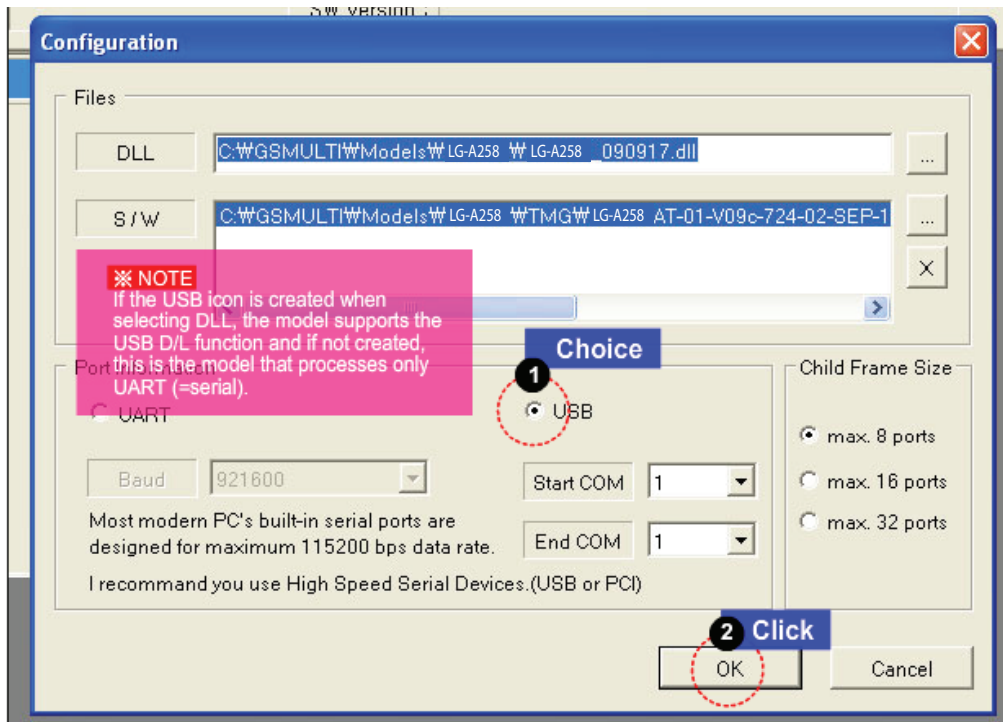
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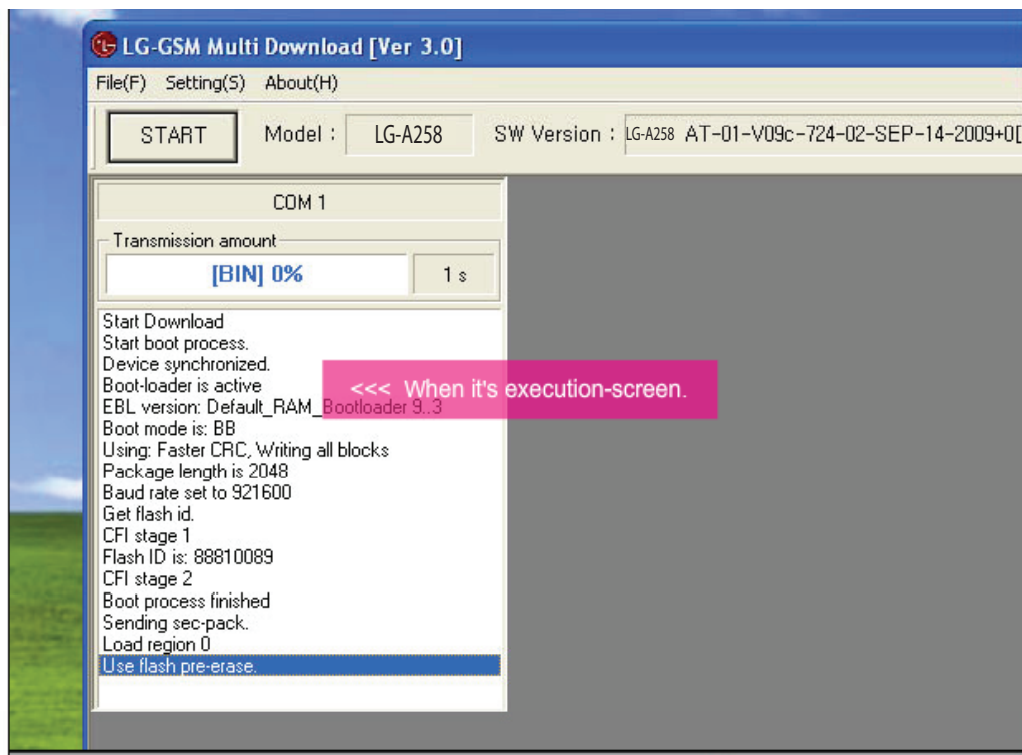
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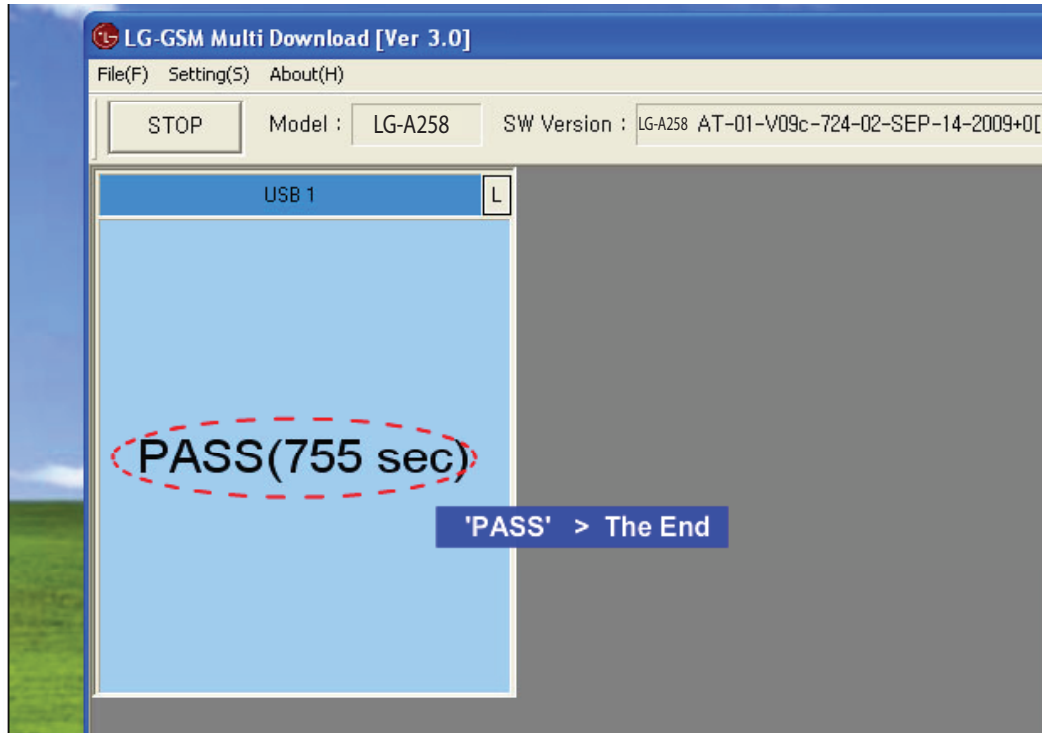
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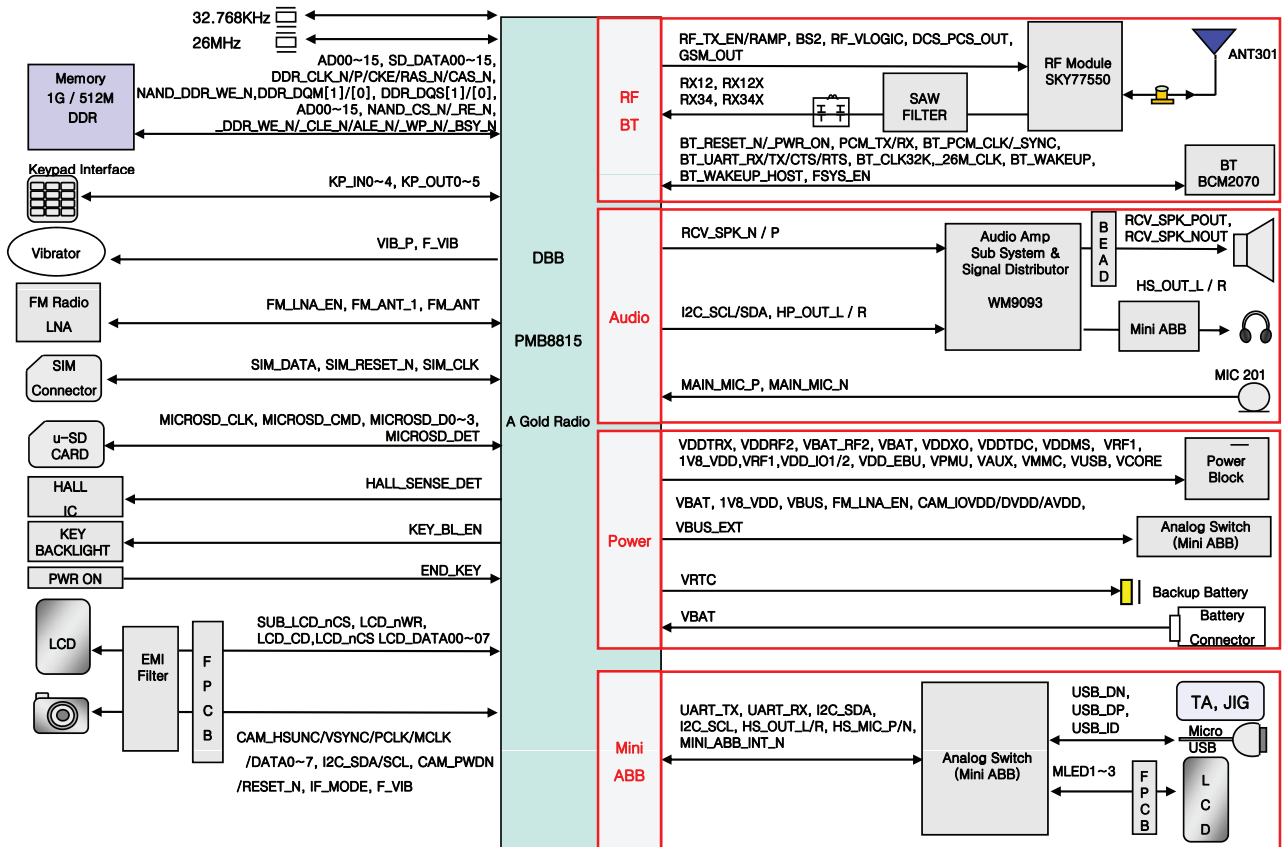
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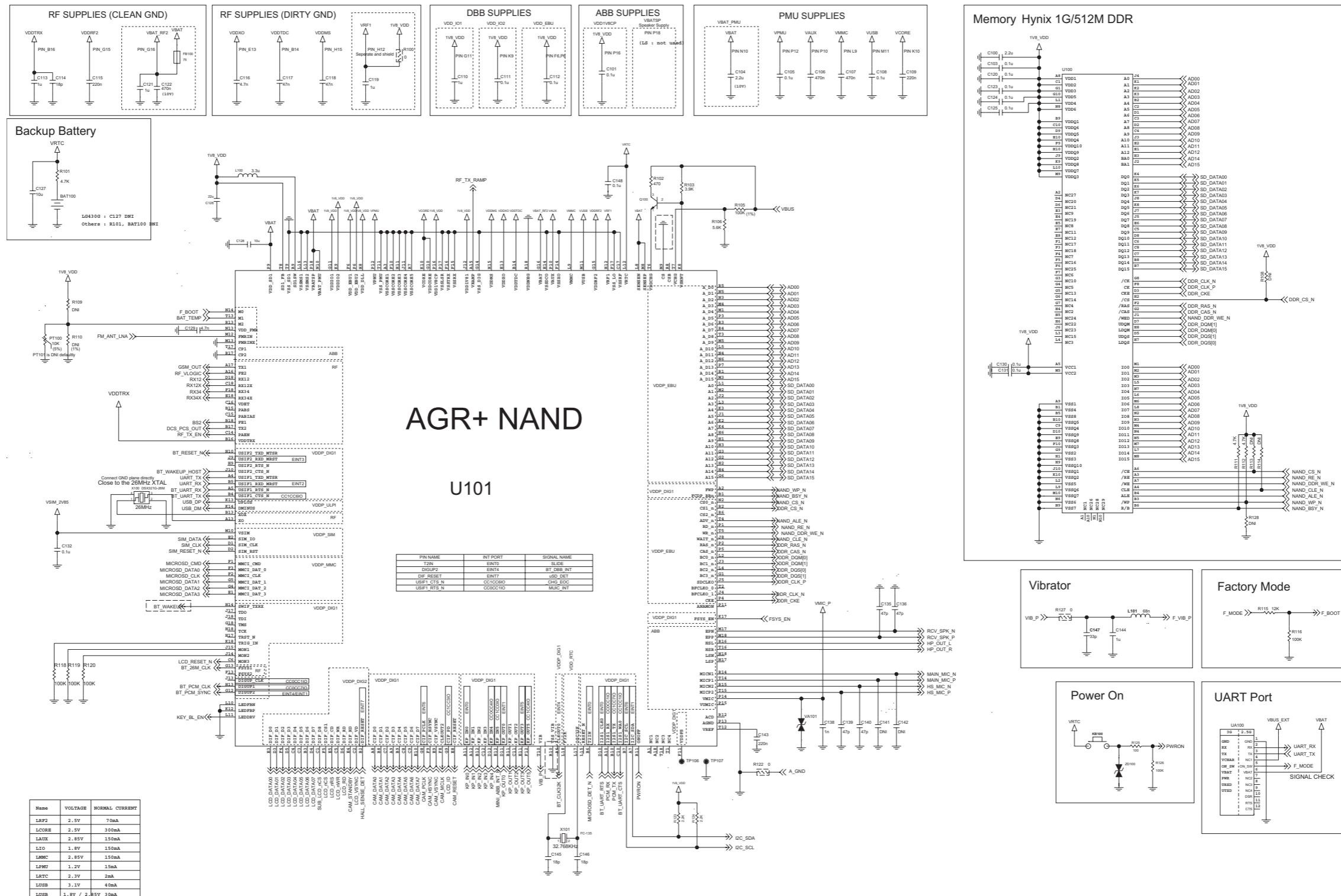
5. DOWNLOAD



6. BLOCK DIAGRAM



7. CIRCUIT DIAGRAM



Audio Subsystem

Microphone

The schematic diagram illustrates a microphone circuit. It features a microphone (MIC200) connected to a network of resistors (R221, R214, R217, R223) and capacitors (C224, C225, C221). The pre-amplifier stage consists of two op-amp buffers, UA218 and UA219, configured as voltage followers. The output of the microphone is connected to the non-inverting input of UA218. The output of UA218 is connected to the non-inverting input of UA219. The output of UA219 is connected to the VMMC_P pin. The circuit is powered by a 1.8V supply (VMMC_P) and a 1.8V supply (VMMC_N). The output of the microphone is connected to the VMMC_P pin. The output of UA218 is connected to the VMMC_P pin. The output of UA219 is connected to the VMMC_P pin. The output of the microphone is connected to the VMMC_P pin. The output of UA218 is connected to the VMMC_P pin. The output of UA219 is connected to the VMMC_P pin.

Mini ABB

Key Backlight

Hall IC

The schematic diagram shows a Hall IC (U201) with the following connections:

- Pin 1 (VDD) is connected to VDD_VDD through a 0.1uF capacitor (C222).
- Pin 2 (VSS) is connected to VSS.
- Pin 3 (VSS) is connected to VSS.
- Pin 4 (GND) is connected to GND.
- Pin 5 (GND) is connected to GND.
- Pin 6 (VDD) is connected to VDD_VDD through a 1uF capacitor (CF19).
- The output of the Hall IC (pin 6) is connected to the Hall_Sense_DET signal.

Battery Connector

[illegible]

KeyPad Interface

The diagram illustrates a 4x5 Keypad Interface circuit. The keypad contains the following buttons:

- NUM 0, NUM 1, NUM 2, NUM 3, NUM 4, NUM 5, NUM 6, NUM 7, NUM 8, NUM 9
- SEND, GO TO, RIGHT, DOWN, CAMERA, UP, CLEAR, LEFT, STAR(*), NUM 12, SHARP(#), NAMES

The circuit is powered by a 5V supply and includes a 10k pull-up resistor. Each row and column is connected to the keypad through a 150 ohm resistor. The keypad is connected to a microcontroller via I2C (SCL, SDA) and a 4-wire UART (TX+, TX-, RX+, RX-).

SIM Connector

[illegible]

RF Part

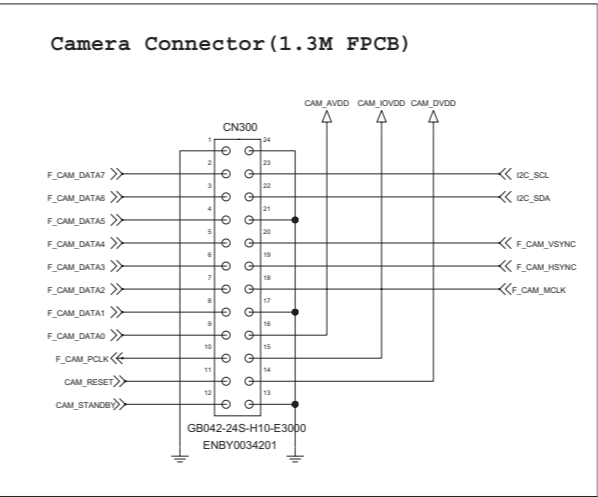
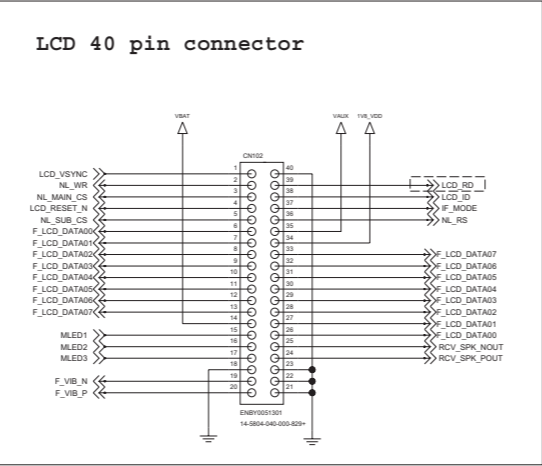
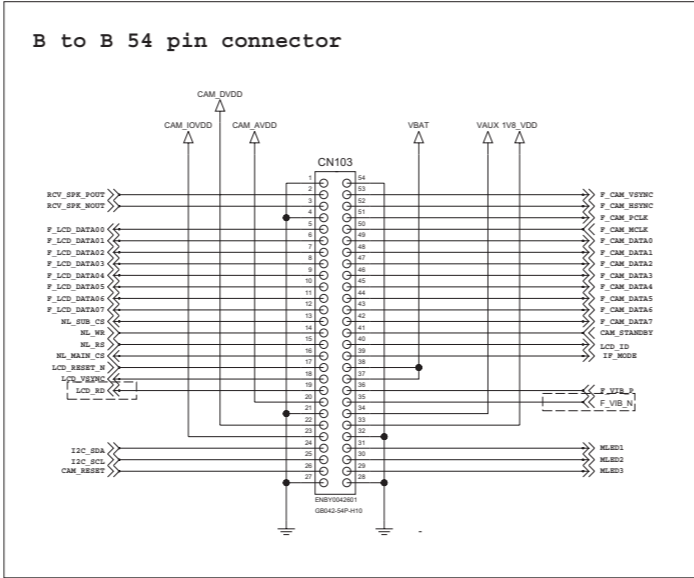
The RF Part schematic diagram illustrates the radio frequency circuitry. It includes three antenna inputs (ANT300, ANT301, ANT302) connected to a series of capacitors (C309, C311, C319, C302, C303) and a switch (SW300). The signal path continues through inductors (L306, L307) and capacitors (C330, C334, C335, C350, C306) to the U301 chip. The U301 chip is connected to various output lines (RX34, RX04X, RX12, RX12X, RF_TX_EN, RF_TX_RAMP, BS2, RF_VLOGIC, DCS_PCS_OUT, GSM_OUT) through a series of inductors (L302, L303, L304, L305, L308, L310, L313, L314, L315) and capacitors (C320, C321, C322, C323, C333, C340). The U301 chip is also connected to a power supply (VDD) and ground (GND) through capacitors (C334, C335, C350, C306).

MODE	RF_VLOGIC	RF_TX_EN	BS2
Standby	LOW	LOW	LOW
RX1	HIGH	LOW	LOW
RX2	HIGH	LOW	HIGH
TX_LB	HIGH	HIGH	LOW
TX_HB	HIGH	HIGH	HIGH

MODE	RF_VLOGIC	RF_TX_EN	BS2
Stanby	LOW	LOW	LOW
RX1	HIGH	LOW	LOW
RX2	HIGH	LOW	HIGH
TX_LB	HIGH	HIGH	LOW
TX_HB	HIGH	HIGH	HIGH

[illegible]

B to B Interface



VOLUME SIDEKEY



8. BGA PIN MAP

BGA IC pin check (U101) - SIM

▪ Ball Diagram (Top View), PMB8815(A-GOLDRADIO+)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T		
		FE1	RK12K	RK12	RK34K	RK24	TMS	TOK	TDI	TRIG_IN	F32K	EPP		VBATSP	VDDNEG	NC3		
18																	18	
17	TX1	TX2	VSSRF			VSSRF		TRST_N	TDO	FSYS_EN	OSC32K	EPN		VSSLSR	CP2		17	
16	FE2	VDDTRK				VSSRF	VBAT				VSSMS			VDD1V8CP	HSL	HSR	16	
15	VRAMP					VSSRF	VDDRF2	VDDMS	MON1		RESET_H				VUMIC	MICN2	MICP2	15
14		VDDTDC	PAEN		VSSRF_D	VSSRF_D	VSSRF_D		MON2	DHINUS				M0	VMIC	MICH1	MICP1	14
13	X0	X0X			VDDX0	FSYS2	FSYS1	DIGUP1		DPLUS	VSSMS	FMRINR	VDD_FMR	AGND		M1		13
12	KP_IN1	KP_IN2	KP_IN3	KP_IN4	KP_IN5	KP_OUT5	DIGUP2	VRP1	VDD1V81	LEDFBP	VRTC	FMRIN		VPMU	ACD	VREF		12
11		KP_OUT1	KP_OUT2	KP_OUT0	KP_OUT3	VDDFS	VDDI01	VSSCORE	VSSCORE		LEDDR	VUSB			ONOFF	VSS_PMU		11
10	I2S1_RX	I2S1_TX	I2S1_WA0	I2S1_CLK0	CIF_D7	VSSCORE	VDDCORE	USIF2_TXD_MTSR	USIF2_OT_S_N	VDDCORE	LEDFBN	VSIM	VBAT_PMU	VAUX	VSS_VIB	VIB		10
9	CIF_D3	CIF_D4	CIF_D6		CIF_VSYN0	CIF_HS_YN0	CIF_PD			VDDI02	VMMC			VDD_SD1	SD1SW	VSS_SD1		9
8	CIF_D0	CIF_D1	CIF_D5		CIF_RESE_T	CLKOUT2	CIF_PCLK	VDD_DLE	WAIT_N	VSHNT	SENSEN	SENSEP				SD1_FB		8
7	I2C_SDA	I2C_SCL	CIF_D2											A_D13	VSSCORE	VCHG		7
6	CLKOUT0	T2IN	MON3	DIF_RD		VDD_EBU	A15	A8					A_D12	VDD_EBU		VDDCHG		6
5	USIF1_RT_S_N	USIF1_RXD_Mrst	DIF_WR	DIF_D3	DIF_CD	DIF_CS1	MMCLDA_T1		SDCLK0			A_D10	A_D9	A_D1	CAS_N	A_D0	WR_N	5
4	USIF1_TXD_MTSR	USIF1_OT_S_N	DIF_D4	DIF_D7	DIF_HD	DIF_D2	MMCLDA_T2	A14	BFCLK0_1	A7	BC2_N	A_D3	A_D11	CKE	A_D7	ADV_N		4
3	VSSCORE	DIF_D6	DIF_D5	DIF_D1	DIF_D0	MMCLDA_T0	A11	A10	BC1_N	A4	A3	A_D15	A_D2	A_D5	A_D6	A_D8		3
2	KP_OUT4	DIF_RESE_T	DIF_VD	CC_RST	CC_IO	MMCLCLK	A12	A13	A2	A6	BC0_N	A1	CS0_N	RAS_N	CS1_N			2
1	NC1	FDDP_RB_N	DIF_D8	CC_CLK	MMCLDA_T3	MMCLCM_D	BC3_N	A9	A5		A0	A_D4		RD_N	A_D14			1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T		

 : not in use

BGA IC pin check (U100) – DDR SDRAM

▪ Ball Diagram (Top View), H8BC50QG0MMR

SDRAM

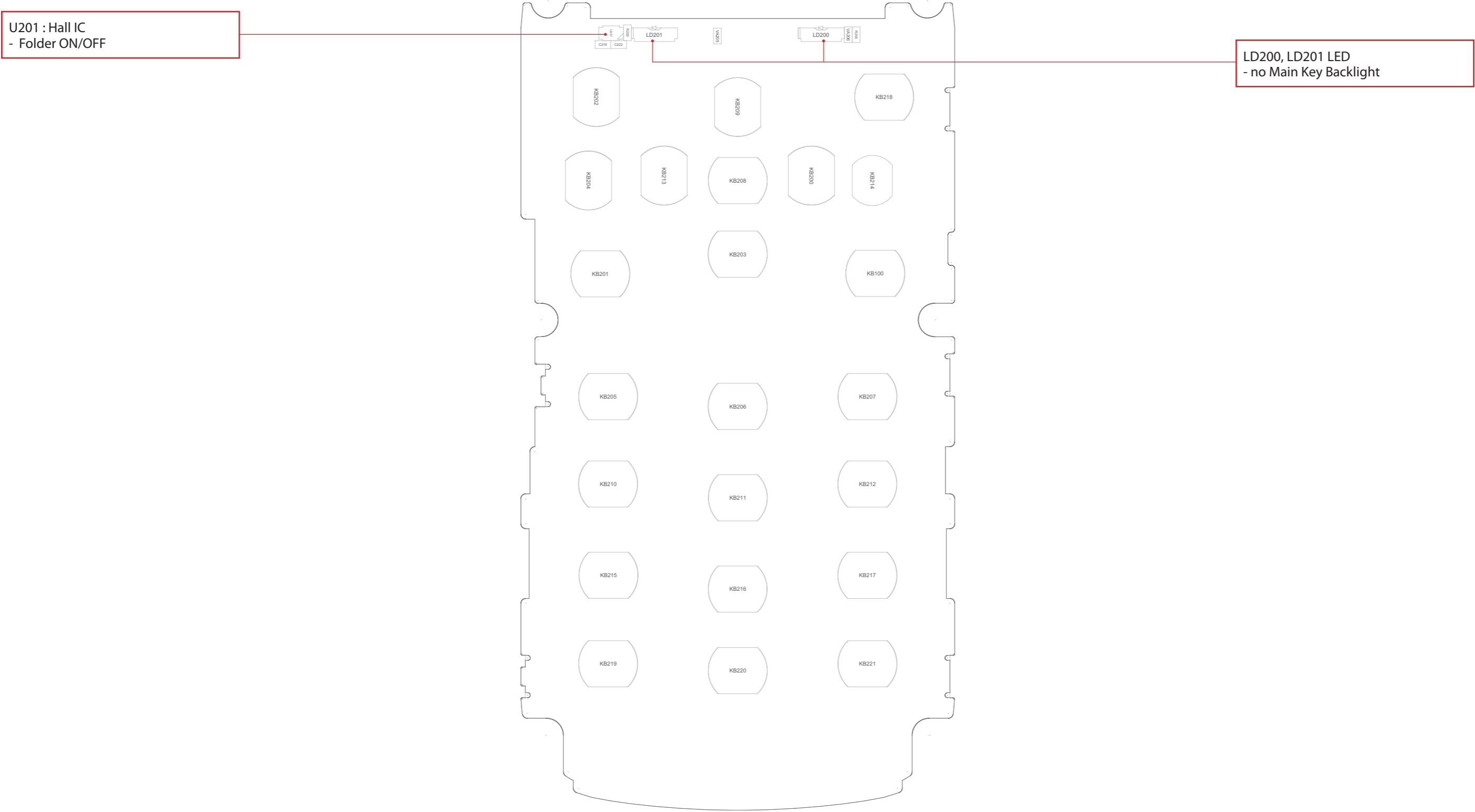
1	2	3	4	5	6	7	8	9	10
NC	NC	/RE	CLE	VCC	/CE	/WE	VDD	VSS	NC
VSS	A4	/WP	ALE	VSS	R/B	DQ15	DQ14	VDDQ	VSSQ
VDD	A5	A7	A9	DQ9	DQ11	DQ13	DQ12	VSSQ	VDDQ
A6	A8	CKE	NC	UDQS	NC	JDQM	DQ10	VDDQ	VSSQ
A12	A11	NC	NC	NC	DQ8	NC	NC	VSSQ	VDDQ
NC	/RAS	NC	NC	NC	NC	NC	CK	VDDQ	VSSQ
VDD	/CAS	NC	NC	NC	NC	NC	/CK	VSS	VDD
VSS	/CS	BA0	NC	NC	NC	LDQS	LDQM	VSSQ	VDDQ
/WE _d	BA1	A10	A0	DQ7	NC	DQ6	DQ4	VDDQ	VSSQ
A1	A2	A3	DQ0	DQ1	DQ2	DQ3	DQ5	VDDQ	VSSQ
VDD	VSS	NC	NC	I/O3	I/O5	I/O14	I/O7	VSSQ	VDDQ
I/O0	I/O1	I/O2	I/O10	VCC	I/O6	I/O13	I/O15	VDDQ	VSSQ
NC	I/O8	I/O9	I/O11	I/O12	VSS	I/O4	VDD	VSS	NC

NAND

DRAM

NC / DNU

9. PCB LAYOUT



LG-A258_MAIN_EAX64107601_1.0_TOP



LG-A258_MAIN_EAX64107601_1.0_BOT

10. STAND ALONE TEST

10.1 Introduction

This manual explains how to examine the status of RX and TX of the model.

A. Tx Test

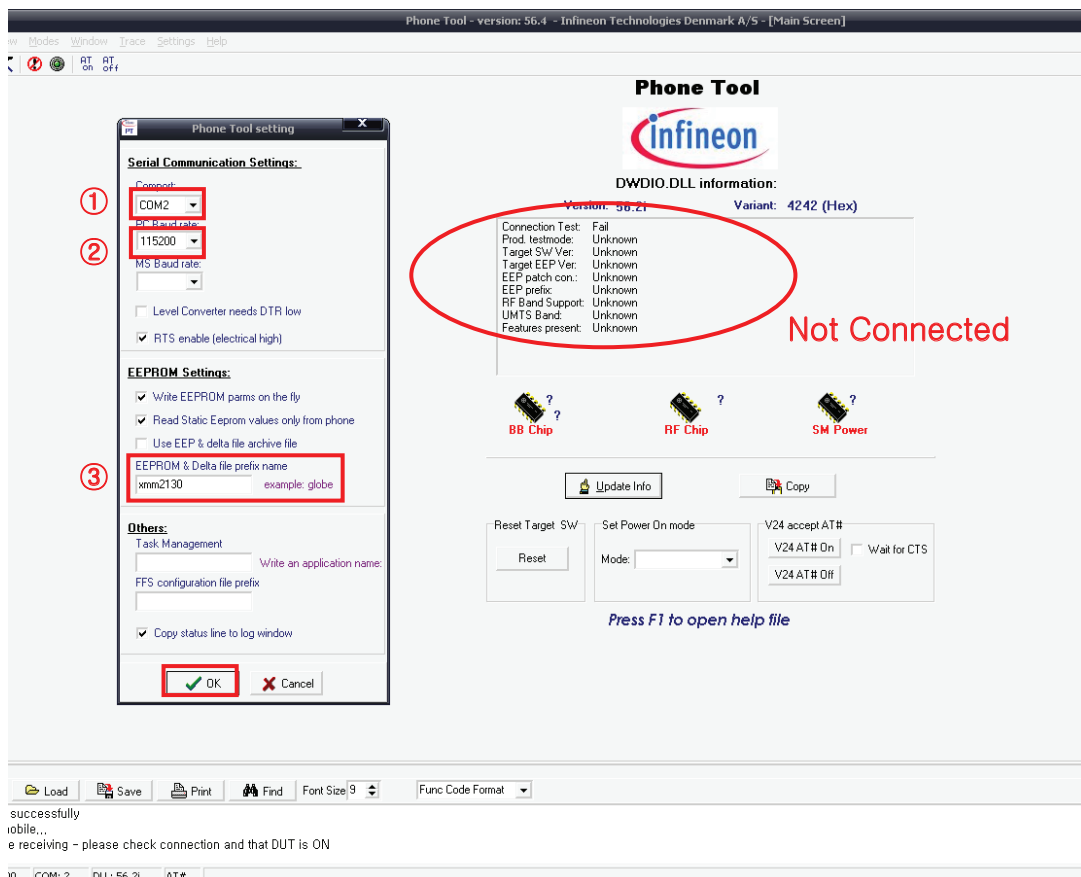
TX test - this is to see if the transmitter of the phones is activating normally.

B. Rx Test

RX test - this is to see if the receiver of the phones is activating normally.

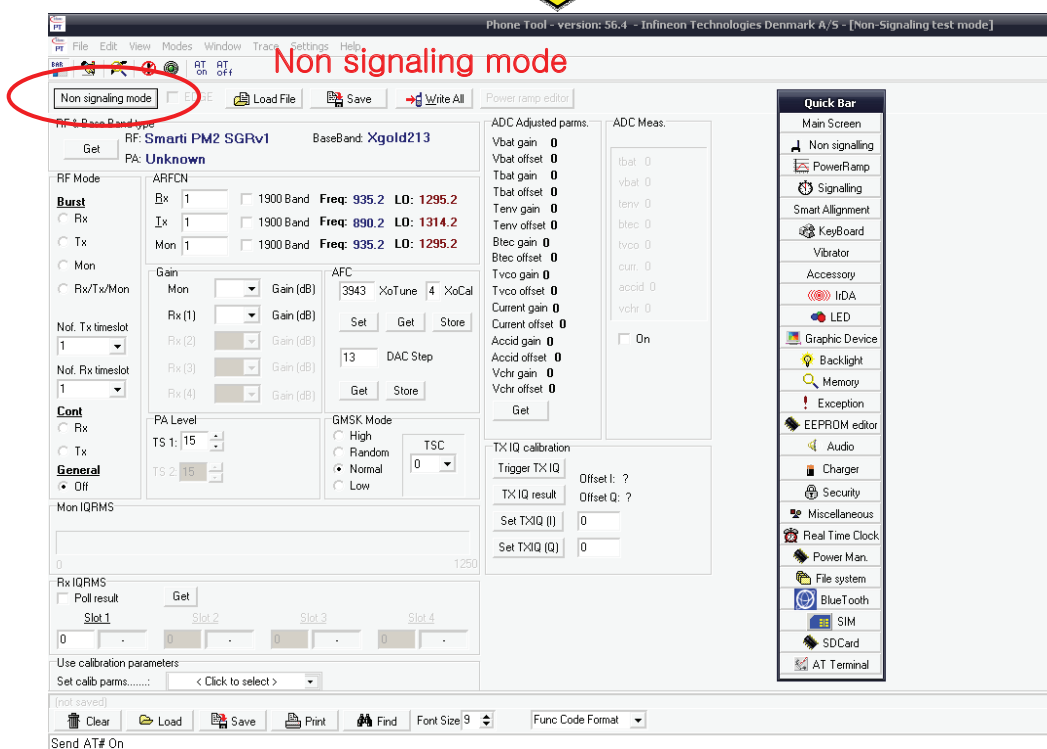
10.2 Setting Method

1. Set COM Port
2. Check PC Baud Rate
3. Confirm EEPROM & Delta file prefix name, and then click "OK".



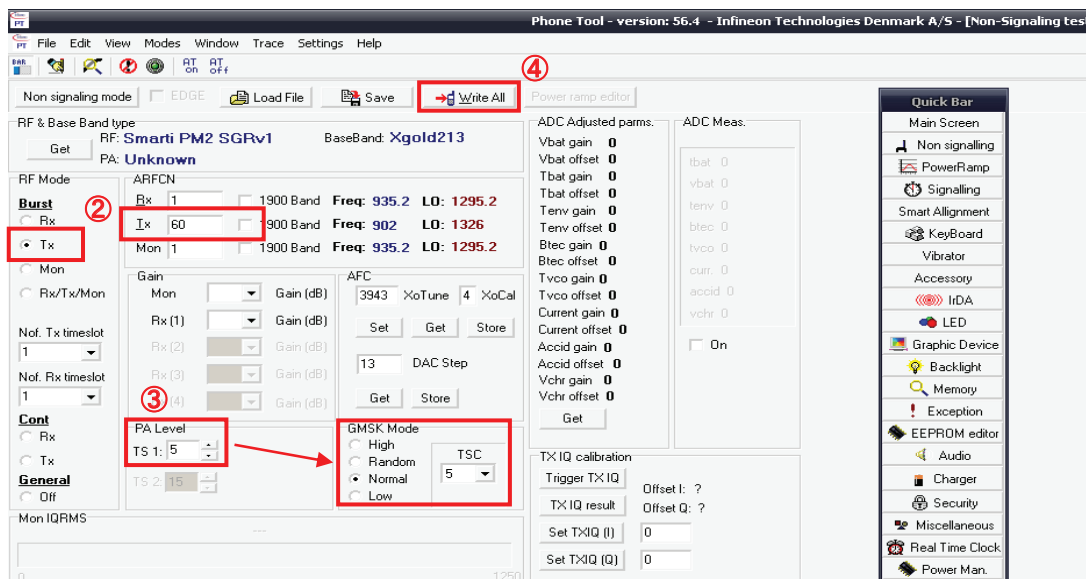
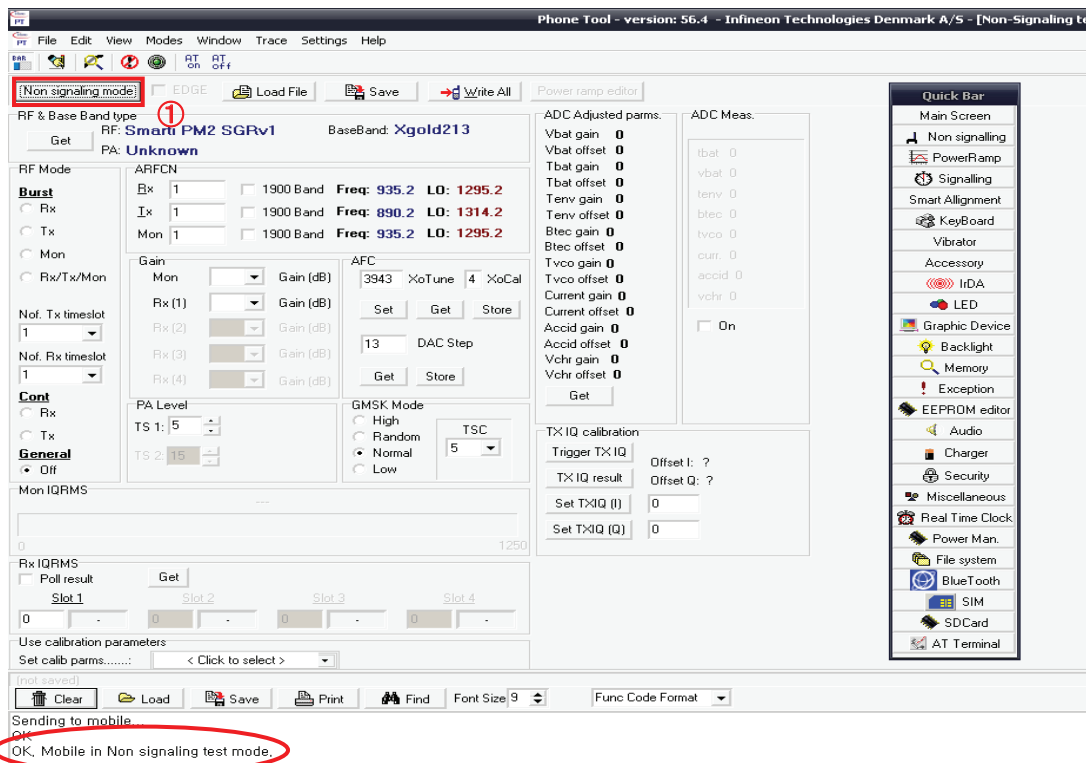
10. STAND ALONE TEST

4. For communicating Phone and Test-Program, click "V24 AT# On" and "Update Info" one by one.
5. For the purpose of the Standalone Test, Change the Phone to "ptest mode" and then Click the "Reset" bar.
6. Select "Non signaling" in the Quick Bar menu. Then Standalone Test setup is finished.



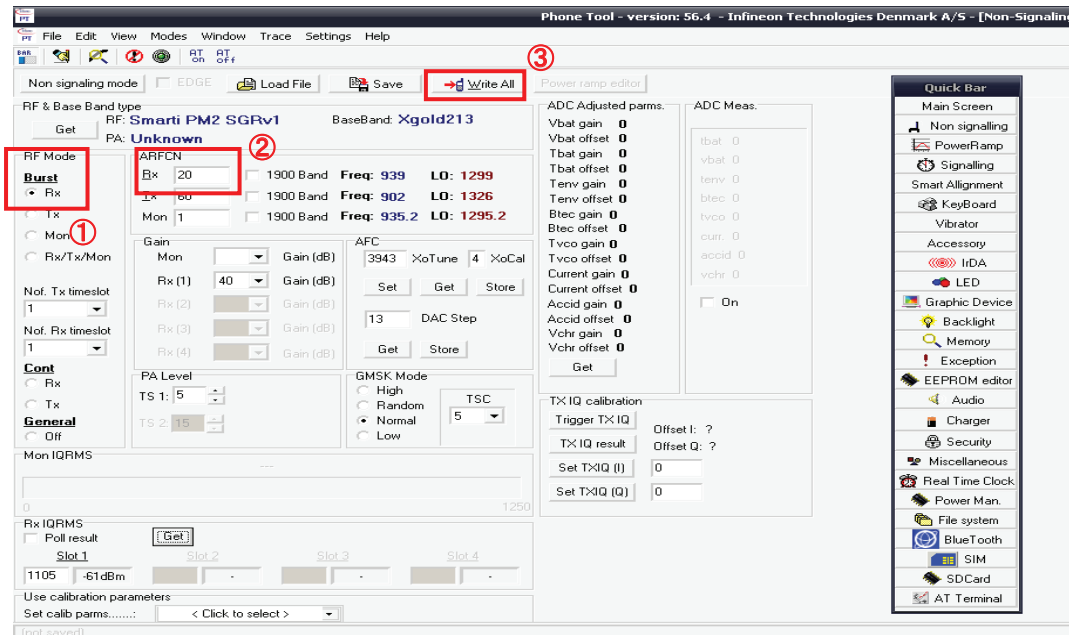
10.3 Tx Test

1. "Non signaling mode" bar and then confirm "OK" text in the command line.
2. Select "Tx" in the RF mode menu and put the number of TX Channel in the ARFCN.
3. Put the number of "PCL" in the PA Level menu.
4. Finally, Click "Write All" bar and try the efficiency test of Phone.

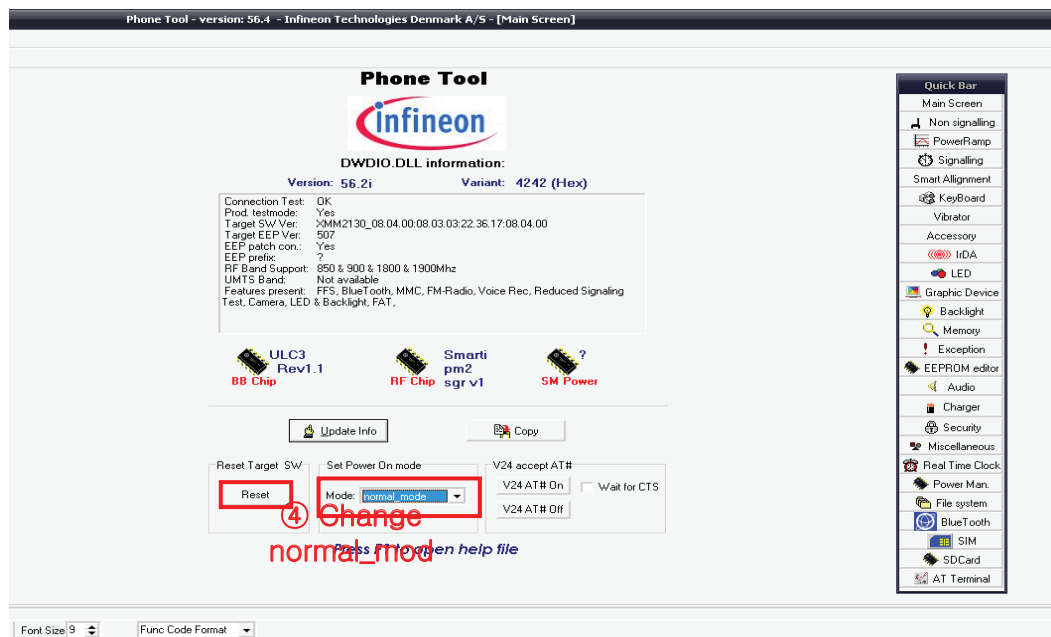


10.4 Rx Test

1. Select "Rx" in the RF mode menu.
2. Put the number of RX Channel in the ARFCN.
3. Finally, Click "Write All" bar and try the efficiency test of Phone.



4. The Phone must be changed "normal mode" after finishing Test.
Change the Phone to "normal mode" and then Click the "Reset" bar.



11.AUTO CALIBRATION

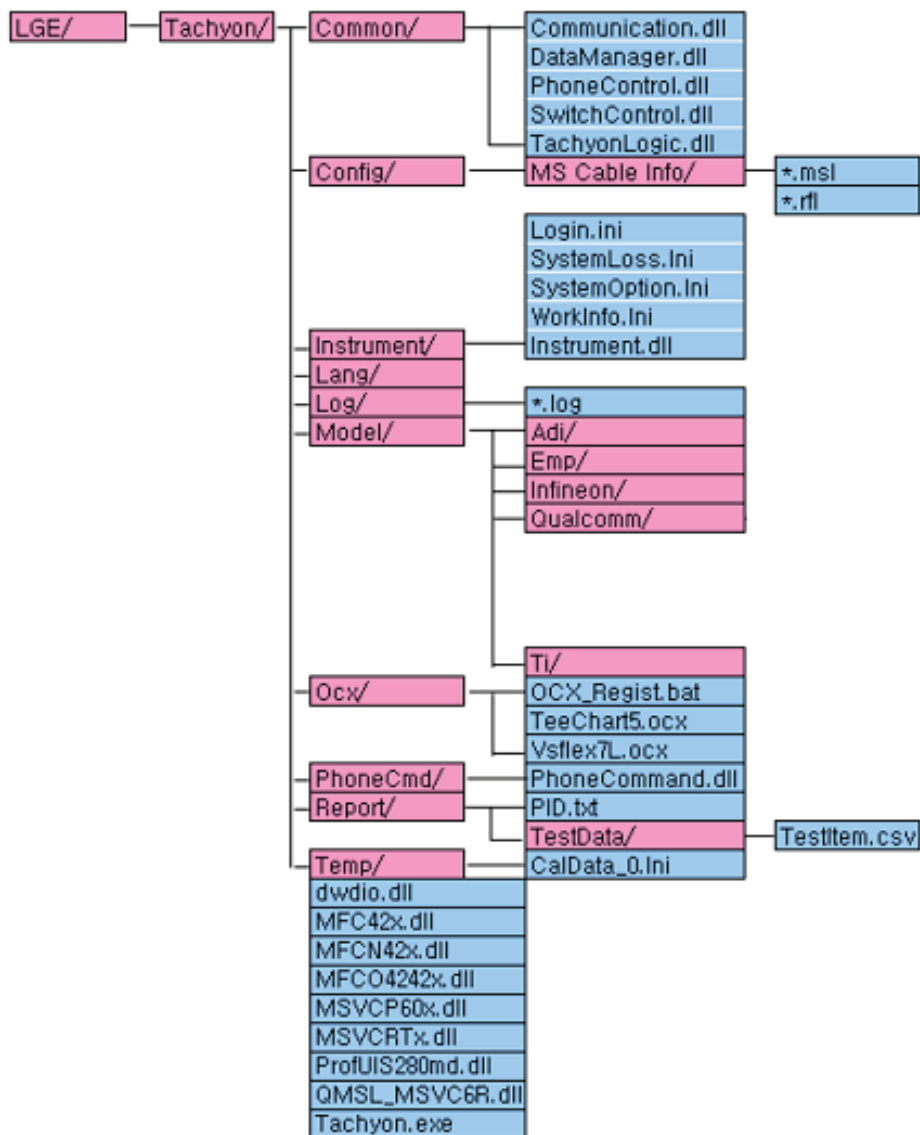
11.1 Overview

Auto-cal (Auto Calibration) is the PC side Calibration tool that perform Tx, Rx and Battery Calibration with Agilent 8960(GSM call setting instrument) and Tektronix PS2521G (Programmable Power supply).

Auto-cal generates calibration data by communicating with phone and measuring equipment then write it into calibration data block of flash memory in GSM phone.

11.2 Directory structure of Tachyon

"CWLGEWTachyon"



11.3 Description of Folder & File.

11.3.1 Folder Explain

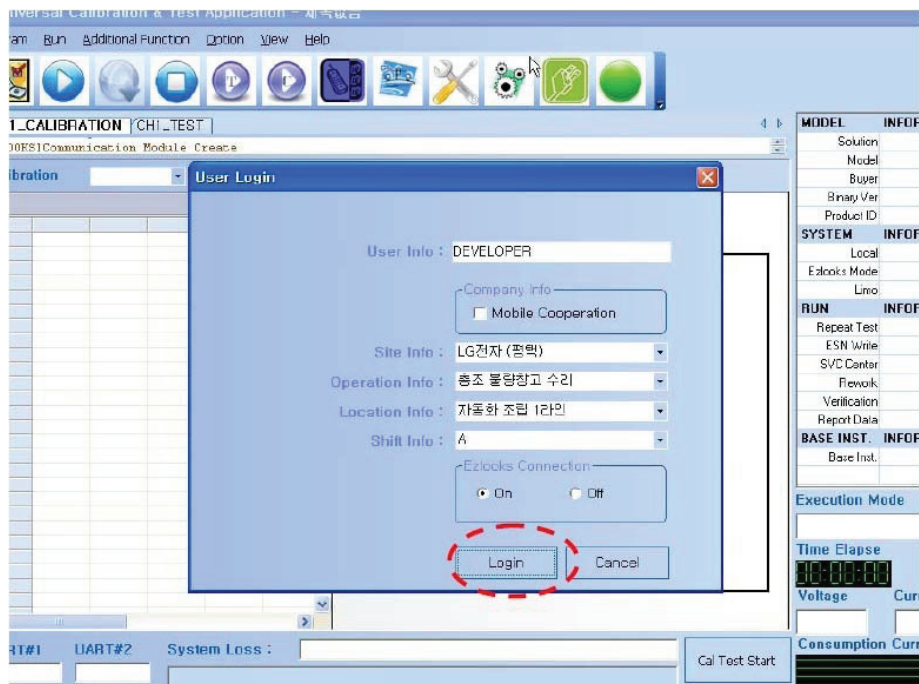
- **Tachyon** : exist tachyon execute file, dll for MFC, dll for UI
- **Common** : common files(XML Data I/O , Auto Test Logic, Tachyon Logic Control), dll for communication with system.
- **Config** : *.ini configuration files for port setting and cable loss.
- **Model** : configuration files for each model.
- **OCX** : component files for Tachyon.
- **PhoneCmd** : files for communication with phone.
- **Report** : test result files.
- **Temp** : store calibration value.

11.3.2 File Explain

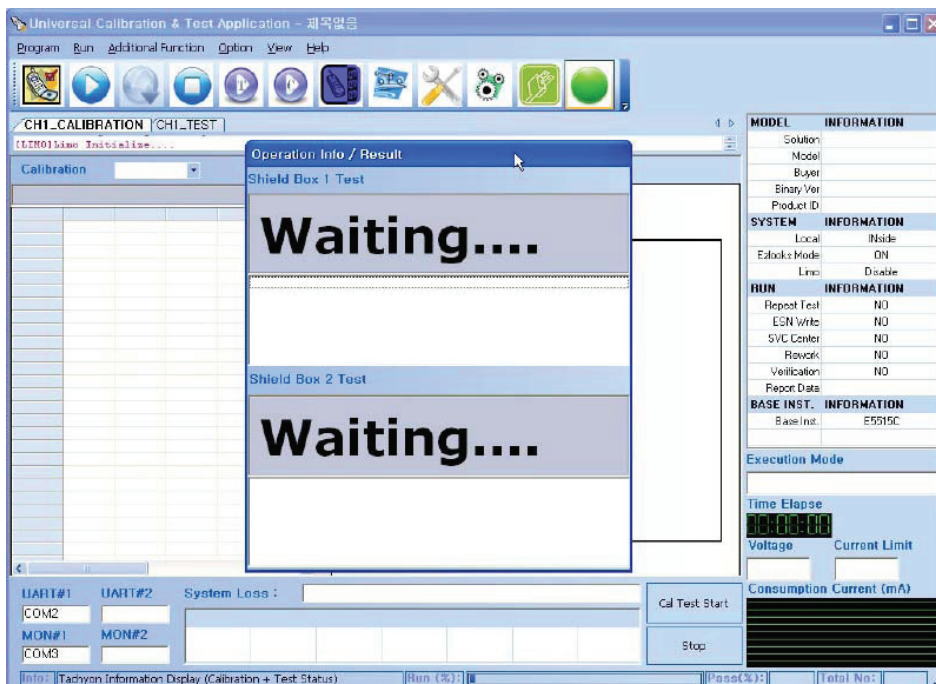
- **Model_Calibration.xml** : stored data for calibration.
- **Model_CallSetuo.xml** : stored equipment setting data for auto test.
- **Model_NV.ini** : default NV data.
- **Model_Sequence.xml** : stored calibration and auto test procedure.

11.4 Procedure

1. Execute "/LGE/Tachyon/Tachyon.Exe" and Click Login button.



2. Tachyon execute ready display



11.5 Tachyon Main UI

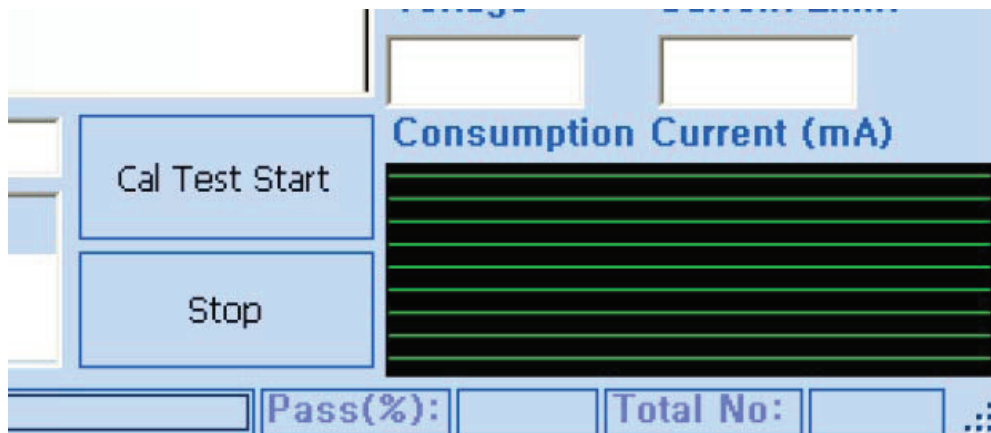
11.5.1 Tool bar



1. Model Selection
2. Calibration + Test
3. Not Support
4. Stop
5. Test Only
6. Calibration Only
7. Phone Control
8. Loss Adjustment
9. System Option
10. Run Option
11. Voltage / Current Setting
12. Show Result

11.5.2 Command button

Only support Calibration Test and Stop button.



11.6 AGC

This procedure is for Rx calibration.

In this procedure, We can get RSSI correction value. Set band EGSM and press Start button the result window will show correction values per every power level and gain code and the same measure is performed per every frequency.

11.7 APC

This procedure is for Tx calibration.

In this procedure you can get proper scale factor value and measured power level.

11.8 ADC

This procedure is for battery calibration.

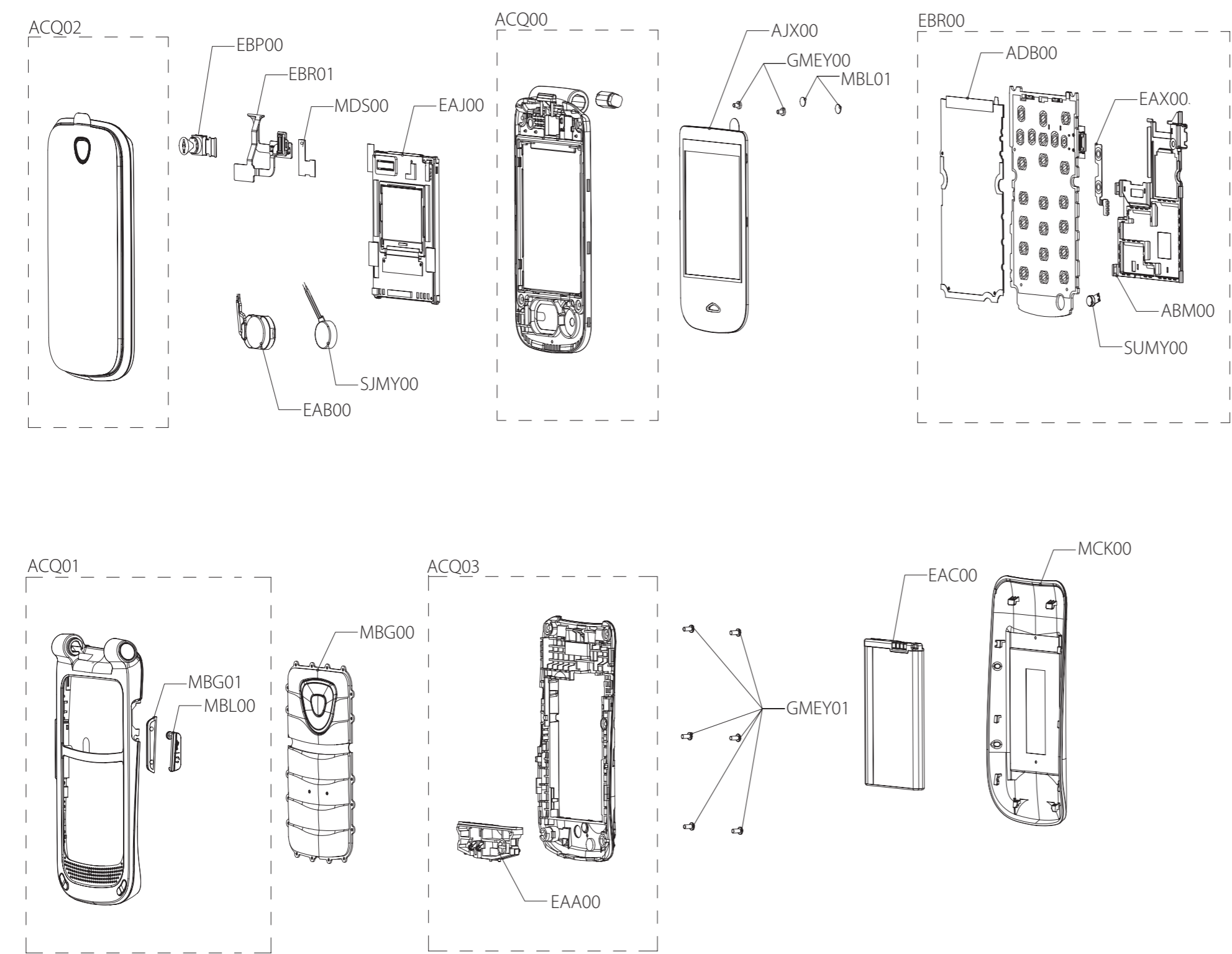
You can get main Battery Config Table and temperature Config Table will be reset.

11.9 Target Power

BAND	Description	Low	Middle	High
GSM 850	Channel	128	191	251
	Frequency	824.2 MHz	836.8 MHz	848.8 MHz
	Max power	32.5 dBm	32.5 dBm	32.5 dBm
EGSM 900	Channel	975	37	124
	Frequency	880.2 MHz	897.4 MHz	914.8 MHz
	Max power	33.0 dBm	33.0 dBm	33.0 dBm
DCS1800	Channel	512	699	885
	Frequency	1710.2 MHz	1747.6 MHz	1784.8 MHz
	Max power	30.0 dBm	30.0 dBm	30.0 dBm
PCS 1900	Channel	512	661	810
	Frequency	1850.2 MHz	1880 MHz	1909.8 MHz
	Max power	29.5 dBm	29.5 dBm	29.5 dBm

12. EXPLODED VIEW & REPLACEMENT PART LIST

12.1 EXPLODED VIEW



Location	Description
EAB00	Speaker,Dual Mode
EAJ00	LCD,Main/Sub Dual Module
ACQ00	Cover Assembly,Upper
EBP00	Camera Module
EBR00	PCB Assembly,Flexible
MBG00	Button
SJMY00	Motor,DC
AJX00	Window Assembly,LCD
ACQ01	Cover Assembly,Lower
ACQ02	Cover Assembly,Front
MBG01	Button
MBL00	Cap,Receptacle
GMEY00	Screw,Machine
MBL01	Cap,Screw
MDS00	Gasket
ACQ03	Cover Assembly,Rear
EAA00	PIFA Antenna,RF
EBR01	PCB Assembly,Main
ABM00	Can Assembly,Shield
SUMY00	Microphone,Condenser
ADB00	Dome Assembly,Metal
EAX00	PCB,Sidekey
GMEY01	Screw,Machine
EAC00	Rechargeable Battery,Lithium Ion
MCK00	Cover,Battery

12. EXPLODED VIEW & REPLACEMENT PART LIST

12.2 Replacement Parts <Mechanic component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	PartNumber	Spec	Remark
1	AGQ000000	Phone Assembly	AGQ86408008	LGA258.ACISTS TS:TITANIUM SILVER -	
2	MEZ002100	Label, Approval	MLAA0062305	COMPLEX KB770 DEUBK ZZ:Without Color -	
2	ACQ100400	Cover Assembly, EMS	ACQ85643506	LGA258.ACISTS TS:TITANIUM SILVER -	
3	ACQ031100	Cover Assembly, Folder	ACQ85438207	LGA258.ACISTS TS:TITANIUM SILVER -	
4	EAB00	Speaker, Dual Mode	EAB62308201	Nd-Fe-B 700mW 8OHM 91DB 720HZ 1812*3.0T wire 15mm DCCA coil WIRE	
4	EAJ00	LCD, Main/Sub Dual Module	EAJ61772501	LM220CM1A QCIF 2.2INCH 176X220 300CD COLOR/MONO 50% 4/3 300:1 60Hz Inverter N - TOVIS	
4	ACQ00	Cover Assembly, Upper	ACQ85454601	LGA250.ABRATS TS:TITANIUM SILVER -	
5	MJN089301	Tape, Window	MJN67772301	COMPLEX LGA250.ABRATS ZZ:Without Color CAMERA	
5	MJN089300	Tape, Window	MJN67772101	COMPLEX LGA250.ABRATS ZZ:Without Color SUB	
5	MKC009400	Window, Camera	MKC63999601	CUTTING PMMA LGA250.ABRATS ZZ:Without Color -	
5	MKC043300	Window, LCD	MKC63999501	MOLD PMMA HI-855M LGA250.ABRATS ZZ:Without Color sub	
6	RAB040100	Film, Inmold	RAB32872701	KR017556 A250 - NISSHA KOREA INC.	
5	MCK084400	Cover, Upper	MCK66690701	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZZ:Without Color -	
6	MET099500	Insert, Nut	MICE0016901	COMPLEX MECH_COMMON ZZ:Without Color -	
5	MCQ009400	Damper, Camera	MCQ66569601	COMPLEX LGA250.ABRATS ZZ:Without Color -	
5	MJN061100	Tape, Protect	MJN67771901	COMPLEX LGA250.ABRATS ZZ:Without Color UPPER	
5	MCQ015701	Damper, Connector	MCQ66570101	COMPLEX LGA250.ABRATS ZZ:Without Color CAMERA	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
5	MCQ049800	Damper, Motor	MCQ66569901	COMPLEX LGA250.ABRATS ZZ:Without Color -	
5	MCQ043300	Damper, LCD	MCQ66569801	COMPLEX LGA250.ABRATS ZZ:Without Color SUB	
4	MEZ000000	Label	MLAZ0038303	COMPLEX LG-LC3200 WA:White PRINTING, PPRI PRINTING	
4	MJN061100	Tape, Protect	MJN67968301	COMPLEX LGA258.ACISTS ZZ:Without Color -	
4	MJB000000	Stopper	MJB62729901	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZZ:Without Color -	
4	MDS000000	Gasket	MDS63757201	COMPLEX LGA250.ABRATS ZZ:Without Color -	
4	EBP00	Camera Module	EBP61341701	LM24HYFF LM24HYFF 2M FF Hynix 1/5", FPC 0deg. 7mm HANSUNG ELCOMTEC CO., LTD.	
4	EBR00	PCB Assembly, Flexible	EBR73680401	LGA250.ABRATS 1.0 Flexible	
5	EBR070400	PCB Assembly, Flexible, SMT	EBR73667001	LGA250.ABRATS 1.0 Flexible	
6	EBR070200	PCB Assembly, Flexible, SMT Bottom	EBR73680801	LGA250.ABRATS 1.0 Flexible	
7	EAG020001	Connector, BtoB	ENBY0042601	GB042-54P-H10 54P 0.40MM STRAIGHT MALE SMD R/TP 1M - LS Mtron Ltd.	
7	EAG020000	Connector, BtoB	ENBY0051301	14-5804-040-000-829+ 40P 0.40MM STRAIGHT MALE SMD R/TP 900mm - KYOCERA ELCO KOREA SALES CO., LTD.	
6	EBR070300	PCB Assembly, Flexible, SMT Top	EBR73680901	LGA250.ABRATS 1.0 Flexible	
7	EAG020000	Connector, BtoB	ENBY0034201	GB042-24S-H10-E3000 24P 0.40MM STRAIGHT SOCKET SMD R/TP 1M - LS Mtron Ltd.	
5	EAX010700	PCB, Flexible	EAX64107701	EAX64107701 LGA250.ABRATS G POLYI Multi 6 0.6 Flexible SI FLEX CO., LTD	
4	MBG00	Button	MBG64402601	MOLD RUBBER SILICON LGA258.ACISTS TA:TITAN PATTERN -	
4	SJMY00	Motor, DC	SJMY0007109	WHVM-1030B15 WHVM-1030B15, 3 V, 80 mA, 10*3.0, 17mm WOOSUNG G&T CO., LTD	
4	AJX00	Window Assembly, LCD	AJX73225101	LGA250.ABRATS ZZ:Without Color -	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
5	MCQ043300	Damper, LCD	MCQ66588201	COMPLEX LGA250.ABRATS ZZ:Without Color MAIN	
5	MKC043300	Window, LCD	MKC63999701	CUTTING PMMA LGA250.ABRATS ZZ:Without Color -	
5	MJN089300	Tape, Window	MJN67772401	COMPLEX LGA250.ABRATS ZZ:Without Color MAIN	
4	ACQ01	Cover Assembly, Lower	ACQ85454701	LGA250.ABRATS ZZ:Without Color -	
5	MJN000001	Tape	MJN67772201	COMPLEX LGA250.ABRATS ZZ:Without Color Motor	
5	MJN009400	Tape, Camera	MJN67771701	COMPLEX LGA250.ABRATS ZZ:Without Color -	
5	MJN000000	Tape	MJN67771601	COMPLEX LGA250.ABRATS ZZ:Without Color RECEIVER	
5	MJN000003	Tape	MJN67756901	COMPLEX LGA250.ABRATS ZZ:Without Color -	
5	MJB000000	Stopper	MJB62709801	MOLD TPU LGA250.ABRATS ZZ:Without Color FOLDER	
5	MCK046000	Cover, Lower	MCK66690801	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZZ:Without Color -	
5	MCE000000	Contact	MCE62253101	PRESS BECU 0.15 LGA250.ABRATS ZZ:Without Color -	
5	MAZ000000	Bracket	MAZ63104701	PRESS STS 304 0.5 LGA250.ABRATS ZZ:Without Color LOWER	
5	MEV000000	Insulator	MEV63879201	COMPLEX LGA250.ABRATS ZZ:Without Color -	
5	RAB150000	MAGNET, SWITCH	MMAA0009601	KF750 VDFBK BK, ZZ, COMPLEX, (empty), 1, , , ,	
5	MEF031100	Hinge, Folder	MHFD0016401	COMPLEX LG-CX280 BLMBK ZZ:Without Color -	
5	MDS000000	Gasket	MDS63746601	COMPLEX LGA250.AFRATS ZZ:Without Color -	
4	ACQ02	Cover Assembly, Front	ACQ85454801	LGA250.ABRATS ZZ:Without Color -	
5	MJN000000	Tape	MJN67881701	COMPLEX LGA250.AFRATS ZZ:Without Color -	
5	MBG01	Button	MBG64206301	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZZ:Without Color -	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
5	MJN061100	Tape, Protect	MJN67772501	COMPLEX LGA250.ABRATS ZZ:Without Color VOLUME	
5	MJB000001	Stopper	MJB62730001	MOLD TPU LGA250.ABRATS ZZ:Without Color -	
5	MJB000000	Stopper	MJB62709901	MOLD TPU LGA250.ABRATS ZZ:Without Color Damper(right) - s190a	
5	MCR000001	Decor	MCR64429801	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZZ:Without Color HINGE RIGHT	
5	MCR000000	Decor	MCR64429701	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZZ:Without Color HINGE LEFT	
5	MCQ000000	Damper	MCQ66570201	COMPLEX LGA250.ABRATS ZZ:Without Color MIKE	
5	MCK032700	Cover, Front	MCK66690901	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZZ:Without Color -	
6	MET099501	INSERT, NUT	MICE0016907	MECH_COMMON ZY, ZZ, PRESS, STS, , , , ,	
6	MET099500	INSERT, NUT	MICE0016912	MECH_COMMON ZY, ZZ, PRESS, STS, , , , ,	
5	MCE000000	Contact	MCE62253201	PRESS BECU 0.15 LGA250.ABRATS ZZ:Without Color -	
5	MBL00	Cap, Receptacle	MBL64898701	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZZ:Without Color -	
4	GMEY00	Screw, Machine	GMEY0010601	GMEY0010601 BH + 1.4mM 2.5mM MSWR FZB N - KUMGANG SCREW CO., LTD	
4	MBL01	Cap, Screw	MBL64898801	COMPLEX LGA250.ABRATS ZZ:Without Color -	
4	MDS00	Gasket	MDS63739501	COMPLEX LGA250.ABRATS ZZ:Without Color -	
3	ACQ03	Cover Assembly, Rear	ACQ85660301	LGA250.AITATS TS:TITANIUM SILVER -	
4	MCQ015700	Damper, Connector	MCQ66588301	COMPLEX LGA250.ABRATS ZZ:Without Color MAIN	
4	MCQ074200	Damper, Speaker	MCQ66588101	COMPLEX LGA250.ABRATS ZZ:Without Color -	
4	MCK063300	Cover, Rear	MCK66691001	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZZ:Without Color EM59	
4	EAA00	PIFA Antenna, RF	EAA62609401	A250-MAIN-KOMA TRIPLE -2DB 3.0 Metal Stamping Type - KOMATECH CO., LTD	
3	EBR01	PCB Assembly, Main	EBR73094108	LGA258.ACISTS 1.0 Main	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
4	EBR071500	PCB Assembly, Main, Insert	EBR73094801	LGA250.ABRATS 1.1 Main	
5	ABM00	Can Assembly, Shield	ABM73516801	LGA250.ABRATS ZZ:Without Color -	
6	MBK070300	Can, Shield	MBK62913501	PRESS STS 304 0.3 LGA250.ABRATS ZZ:Without Color -	
6	MHK000000	Sheet	MHK63526901	COMPLEX LGA250.ABRATS ZZ:Without Color -	
6	MEZ000900	Label, After Service	MLAB0001102	COMPLEX C2000 CGRSV WA:White C2000 USASV DIA 4.0 PRINTING,	
5	SUMY00	Microphone, Condenser	SUMY0003815	B4010AL443-49 -44DB 2.2KOHM OMNI 1.1TO10V 4x1.0t FPCB GoerTek Inc.	
5	MEV000000	Insulator	MEV63878301	COMPLEX LGA250.ABRATS ZZ:Without Color -	
5	MEV000001	Insulator	MEV63972201	CUTTING PET LGA250.AITATS ZZ:Without Color -	
5	ADB00	Dome Assembly, Metal	ADB73598301	LGA250.ABRATS ZZ:Without Color -	
5	RAA050100	Resin, PC	BRAH0001301	UF-1060	
5	EAX00	PCB, Sidekey	EAX64107801	LGA250.ABRATS D POLYI Double Double - Sidekey	
4	EBR071800	PCB Assembly, Main, SMT	EBR73095209	LGA258.ACISTS 1.1 Main	
5	MEZ000000	Label	MLAZ0038301	COMPLEX LG-VX6000 ZZ:Without Color PID Label 4 Array PRINTING,	
5	EBR071700	PCB Assembly, Main, SMT Top	EBR73095501	LGA250.ABRATS 1.0 Main	
6	EAX010000	PCB, Main	EAX64107601	LGA250.ABRATS E FR-4 Build-Up 6 0.8 Main	
5	EBR071600	PCB Assembly, Main, SMT Bottom	EBR73095405	LGA258.ATHATS 1.1 Main	
3	GMEY01	Screw, Machine	GMEY0011201	GMEY0011201 BH + 1.4mM 3mM MSWR FZB N N LG ELECTRONICS INC.	
1	AGF000000	Package Assembly	AGF76259401	LGA258.ACISTS ZZ:Without Color LG-A258 CIS(EU1/CIS_UB/CIS_LB_China/720EA)	
2	MAY047100	Box, Master	MBEE0061001	COMPLEX GD510.ACZESV ZZ:Without Color EU1 Master Box	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
2	MEZ047200	Label, Master Box	MLAJ0004402	PRINTING CG300 CGR DG ZZ:Without Color LABEL MASTER BOX(for CGR TDR 2VER. mbox_label) GSM standard_master box label	
2	MEZ084100	Label, Unit Box	MLAQ0018301	PRINTING GS200 CISBK ZZ:Without Color Unit Box Label(CIS USE-LGE-Peel-90*40) CIS only_Koerea_Peel_unit box label_90*40	
2	MAF086500	Bag, Vinyl	MBAD0005204	COMPLEX LG-LX260 SPRAG ZZ:Without Color -	
2	MAY084000	Box, Unit	MAY65229101	BOX Paper 120 56 90 5 COLOR LGA258.ACISTS ZZ:Without Color LG-A258 CIS Unit Box(EU1/Russian+Kajak+UKR)	
2	MEZ000000	Label	MLAZ0050901	COMPLEX KU990.AGBRBK ZZ:Without Color Battery Warning Label (Lithium ion Battery Label)	
2	AGJ000000	Pallet Assembly	APLY0003911	GT540.ACISBK ZZ:Without Color EU1 TYPE_CIS_CIS Body(SW)+Cap(EU)+AL_720ea	
3	MAY010800	Box, Carton	MBEC0003604	COMPLEX GX300.ACISWR ZZ:Without Color EU1 CIS Body(720ea/H:605mm)	
3	MCCL00	Cap, Box	MCCL0002501	COMPLEX GD510 CZESV ZZ:Without Color -	
3	MPCY00	Pallet	MPCY0012403	COMPLEX KG800 FRABK DB:DARK BLUE -	
1	AAD000000	Addition Assembly	AAD85691108	LGA258.ACISTS TS:TITANIUM SILVER -	
2	MCK00	Cover, Battery	MCK66691101	MOLD PC LUPOY SC-1004A LGA250.ABRATS ZY:Color Unfixed -	

12. EXPLODED VIEW & REPLACEMENT PART LIST

12.2 Replacement Parts <Main component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	PartNumber	Spec	Remark
6	C219, C222	Capacitor, Ceramic, Chip	ECZH0003103	GRM36X7R104K10PT 100nF 10% 10V X7R - 55TO+125C 1005 R/TP - MURATA MANUFACTURING CO., LTD.	
6	LD200, LD201	LED, Chip	EDLH0015107	99-218UMC/2229397/TR8 WHITE 2.95~3.25 30mA 1200~1600mcd x, y 110mW - R/TP 2P - EVERLIGHT ELECTRONICS CO., LTD.	
6	R203, R204	Resistor, Chip	ERHZ0000483	MCR01MZP5J470 47OHM 5% 1/16W 1005 R/TP - ROHM.	
6	U201	IC, Hall Effect Switch	EUSY0419501	S-5712ACDL 2.5V to 3.3 - SNT R/TP 4P - SEIKO INSTRUMENTS INC	
6	VA205, VA206	Varistor	SEVY0003901	EVL5M02200 5.5V 0% 480F 1.0*0.5*0.6 NONE SMD R/TP AMOTECH CO., LTD.	
6	U202	IC, Mini ABB	EAN62112401	RT8966AGQW RT8966A 1.65~5.5V 60uA SWITCH/MULTIPLEXER QFN R/TP 32P Mini ABB MUIC, Charger IC, Current Sink 4Ch, LDO 4Ch RICHTEK TECHNOLOGY CORP. QFN R/TP 32P RICHTEK TECHNOLOGY CORP.	
6	C309	Capacitor, Ceramic, Chip	ECZH0000802	C1005C0G1H010CT 1pF 0.25PF 50V NP0 - 55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	C353	Inductor, Multilayer, Chip	ELCH0001048	1005GC2T10NJLF 10NH 5% - 250mA 0.42OHM 2.5GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	
6	FL302, FL305, FL306	Filter, EMI/Power	SFEY0015501	ICVE10184E050R101FR ESD/EMI 550HZ 10F 0H SMD R/TP INNOCHIPS TECHNOLOGY	
6	FL303, FL304, FL307	Filter, EMI/Power	SFEY0012501	ICVE10054E250R201FR ESD/EMI 0HZ 25pF 0H SMD R/TP INNOCHIPS TECHNOLOGY	
6	C311, C352	Capacitor, Ceramic, Chip	ECZH0000813	C1005C0G1H101JT 100pF 5% 50V NP0 -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	C344	Capacitor, Ceramic, Chip	ECZH0001202	C1005Y5V1C223ZT 22nF -20TO+80% 16V Y5V - 30TO+85C 1005 R/TP - TDK KOREA COOPERATION	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
6	C303	Inductor, Multilayer, Chip	ELCH0004708	1005GC2T2N7SLF 2.7NH 0.3NH - 300mA 0.17OHM 5.5GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	
6	R242	Resistor, Chip	ERHZ0000405	MCR01MZP5J103 10KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	R243	Resistor, Chip	ERHZ0000401	MCR01MZSJ000 0OHM 5% 1/16W 1005 R/TP - ROHM.	
6	VA218, VA219	Varistor	SEVY0004201	ICVS0514X350FR 14V 0% 120F 1.0*0.5*0.55 NONE SMD R/TP INNOCHIPS TECHNOLOGY	
6	C219, C222	Capacitor, Ceramic, Chip	ECZH0003103	GRM36X7R104K10PT 100nF 10% 10V X7R - 55TO+125C 1005 R/TP - MURATA MANUFACTURING CO., LTD.	
6	C135, C136, C139, C140, C202, C203, C225, C238, L308, L313	Capacitor, Ceramic, Chip	ECCH0000122	MCH155A470JK 47pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C126	Capacitor, Ceramic, Chip	ECZH0025502	GRM219R60J226M 0.000022F 20% 6.3V X5R - 55TO+85C 2012 R/TP 0.85MM MURATA MANUFACTURING CO., LTD.	
6	R200, R201, R202, R205, R209, R211, R212, R213, R215, R216, R218, R219, R220	Resistor, Chip	ERHZ0000420	MCR01MZP5J151 150OHM 5% 1/16W 1005 R/TP - ROHM.	
6	R111, R112, R316	Resistor, Chip	ERHZ0000485	MCR01MZP5J472 4.7KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C127, C221	Capacitor, Ceramic, Chip	ECCH0005604	GRM188R60J106M 10000000 pF, 6.3V, M, X5R, TC, 1608, R/TP, 0.8 mm MURATA MANUFACTURING CO., LTD.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
6	R229, R230, R232, R233, R234	Resistor, Chip	ERHZ0000486	MCR01MZP5J473 47KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	R123, R124, R217, R223, R235	Resistor, Chip	ERHZ0000443	MCR01MZP5J222 2.2KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C236, C254, C314, C315, C324	Capacitor, Ceramic, Chip	ECCH0000110	MCH155A100D 10pF 0.5PF 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C313, C317, C318	Capacitor, Ceramic, Chip	ECCH0000155	MCH153CN103KK 10nF 10% 16V X7R -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	R116, R118, R119, R120, R126, R210, R244, R307, R309	Resistor, Chip	ERHZ0000406	MCR01MZP5J104 100KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	R105, R226, R228, R318	Resistor, Chip	ERHZ0000204	MCR01MZP5F1003 100KOHM 1% 1/16W 1005 R/TP - ROHM.	
6	C147, C321, C322, C334	Capacitor, Ceramic, Chip	ECZH0000830	C1005C0G1H330JT000F 33pF 5% 50V NP0 -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	C109, C115, C143, C204, C205, C210, C211	Capacitor, Ceramic, Chip	ECZH0001216	C1005X5R1A224KT000E 220nF 10% 10V X5R -55TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	C110, C113, C119, C144, C347	Capacitor, Ceramic, Chip	ECCH0004904	GRM155R60J105K 1uF 10% 6.3V X5R -55TO+85C 1005 R/TP - MURATA MANUFACTURING CO., LTD.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
6	C100, C230, C312, C316, C335	Capacitor, Ceramic, Chip	ECCH0007804	CL05A225MP5NSNC 2.2uF 20% 10V X5R - 55TO+85C 1005 R/TP 0.5MM SAMSUNG ELECTRO- MECHANICS CO., LTD.	
6	R241	Resistor, Chip	ERHY0000105	MCR01MZP5F51R0 51OHM 1% 1/16W 1005 R/TP - ROHM.	
6	C121, C206, C207, C231, C239, C240, C246, C255, C342, C345, C351	Capacitor, Ceramic, Chip	ECZH0001215	C1005X5R1A105KT000F 1uF 10% 10V X5R - 55TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	Q301	TR, Bipolar	EQBN0019201	KTC3770V NPN 3V 20V 12V 100mA 999A 999 100mW VSM R/TP 3P KEC CORPORAITION	
6	R225	Resistor, Chip	ERHZ0000206	MCR01MZP5F10R0 10OHM 1% 1/16W 1005 R/TP - ROHM.	
6	C212, C213, C214, C216, C217, C241, C341	Capacitor, Ceramic, Chip	ECCH0000198	CL05A225MQ5NSNC 2.2uF 20% 6.3V X5R - 55TO+85C 1005 R/TP . SAMSUNG ELECTRO- MECHANICS CO., LTD.	
6	U100	IC, MCP, NAND	EUSY0425901	H8BCS0QG0MMR-46M NAND/1G SDRAM/512M 0VTO0V 8.0x9.0x1.0 TR 130P NAND+DRAM BGA - HYNIX SEMICONDUCTOR INC.	
6	C128	Capacitor, Ceramic, Chip	ECCH0007803	CL10A106MP8NNNC 10uF 20% 10V X5R -55TO+85C 1608 R/TP 0.8MM SAMSUNG ELECTRO- MECHANICS CO., LTD.	
6	FB300	Filter, Bead	SFBH0006806	CIM05J601NC 600 ohm 1.0X0.5X0.5 25% 0.6 ohm 0.3A SMD R/TP 2P 0 SAMSUNG ELECTRO- MECHANICS CO., LTD.	
6	C249, C250, C251, C320	Capacitor, Ceramic, Chip	ECCH0000120	MCH155A390J 39pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C300, C307	Inductor, Multilayer, Chip	ELCH0001405	LL1005-FHL3N3S 3.3NH 0.3NH - 400mA 0.16OHM 9.1GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TOKO, INC.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
6	FB202, FB204, FB205, FB206	Filter, Bead	SFBH0008101	BLM15AG601SN1D 600 ohm 1.0X0.5X0.5 25% 0.6 ohm 0.3A SMD R/TP 2P 0 MURATA MANUFACTURING CO., LTD.	
6	U101	IC, Digital Baseband Processor, GSM	EUSY0429401	PMB8815 , 281, EDGE Rx, ARM11 208MHz, NAND booting, 2.0Mp, FMR, IC, Digital Baseband Processor BGA R/TP 281P INFINEON TECHNOLOGIES (ASIA PACIFIC) PTE LTD.	
6	R100, R122, R127, R301	Wire Pad, Short	SAFP0000501	LG-VS760 VRZ	
6	Q100, Q200	TR, Bipolar	EQBN0020501	KTC4075E NPN 5V 60V 50V 150mA 100NA 700 100mW ESM R/TP 3P KEC CORPORAITION	
6	C229, C237	Capacitor, Ceramic, Chip	ECCH0000117	CL05C270JB5NNNC 27pF 5% 50V NP0 -55TO+125C 1005 R/TP 0.5 SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	D203, D204, D205, VA208, VA209, VA230, VA305, ZD100, ZD200	Diode, TVS	EDTY0009401	VMNZ6.8CST2R 5.5V 0 10V 0A 200mW SC70 R/TP 6P 5 ROHM.	
6	C106, C107, C348, C349	Capacitor, Ceramic, Chip	ECZH0001217	GRM155R60J474K 470nF 10% 6.3V X5R -25TO+70C 1005 BK-DUP - MURATA MANUFACTURING CO., LTD.	
6	FB200, FB201	Filter, Bead	EAM62150501	CIC10J601NC_ 600 ohm 1.6X0.8X0.8 25% 0.15 ohm 0.75A SMD R/TP 2P 0 SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	R313	Resistor, Chip	ERHZ0000531	MCR01MZP5J271 270OHM 5% 1/16W 1005 R/TP - ROHM.	
6	L200	Inductor, Multilayer, Chip	ELCH0001556	LL1608-FSLR27J 270NH 5% - 150mA - - 3.5OHM 470MHZ 8 SHIELD NONE 1.6X0.8X0.8MM R/TP TOKO, INC.	
6	C337, C338	Capacitor, Ceramic, Chip	ECCH0000129	MCH155A121JK 120pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	R102	Resistor, Chip	ERHZ0000484	MCR01MZP5J471 470OHM 5% 1/16W 1005 R/TP - ROHM.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
6	VA205, VA206	Varistor	SEVY0003901	EVL5M02200 5.5V 0% 480F 1.0*0.5*0.6 NONE SMD R/TP AMOTECH CO., LTD.	
6	C104	Capacitor, Ceramic, Chip	ECCH0005603	GRM188R61A225K 2.2uF 10% 10V X5R -55TO+85C 1608 R/TP - MURATA MANUFACTURING CO., LTD.	
6	R312	Resistor, Chip	ERHZ0000449	MCR01MZP5J243 24KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C114, C145, C146	Capacitor, Ceramic, Chip	ECCH0000113	MCH155A180J 18pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C325	Capacitor, Ceramic, Chip	ECZH0001002	C1005CH1H0R5BT000F 0.5pF 0.1PF 50V NP0 - 55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	R103	Resistor, Chip	ERHZ0000475	MCR01MZP5J392 3.9KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	U200	IC, Audio Sub System	EUSY0403901	WM9093ECS/R 1.71~5.5V 0W WLCSP R/TP 20P - WOLFSON MICROELECTRONICS PLC	
6	C326	Inductor, Multilayer, Chip	ELCH0004701	1005GC2T12NJLF 12NH 5% - 250mA 0.48OHM 2.1GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	
6	C232, C234, C243, C245	Capacitor, Ceramic, Chip	ECCH0000115	MCH155A220JK 22pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C350	Capacitor, Ceramic, Chip	ECCH0000104	MCH155A030C 3pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C138, C253, C331, C332, L314, R314	Capacitor, Ceramic, Chip	ECCH0000143	MCH155CN102KK 1nF 10% 50V X7R -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	R227	Resistor, Chip	ERHY0000254	MCR01MZP5J472 4.7KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	R208	Resistor, Chip	ERHZ0000412	MCR01MZP5J122 1.2KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	R311	Resistor, Chip	ERHZ0003801	MCR01MZP5J5R1 5.1OHM 5% 1/16W 1005 R/TP - ROHM.	
6	L316	Inductor, Multilayer, Chip	ELCH0005004	HK1005 22NJ 22NH 5% - 300mA 0.6OHM 1.9GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO., LTD	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
6	R224	Resistor, Chip	ERHZ0000295	MCR01MZIP5F5102 51KOHM 1% 1/16W 1005 R/TP - ROHM.	
6	FL300	Filter, Saw, Dual	EAM62071301	B9836 GSM QUAD 1.8*1.4*0.4 SMD R/TP 10P EPCOS PTE LTD.	
6	C117, C118, C343	Capacitor, Ceramic, Chip	ECCH0002002	C1005X7R1A473KT000F 47000pF 10% 10V Y5P - 30TO+85C 1005 R/TP - TDK CORPORATION	
6	R221, R222	Resistor, Chip	ERHZ0000201	MCR01MZIP5F1000 100OHM 1% 1/16W 1005 R/TP - ROHM.	
6	R206, R207	Resistor, Chip	ERHZ0000240	MCR01MZIP5F20R0 20OHM 1% 1/16W 1005 R/TP - ROHM.	
6	U301	Module, Tx Module	SMRH0007101	SKY77550 33DBM, 33DBM, 31DBM, 31DBM 30DB, 30DB, 28DB, 28DB 39%, 39%, 37%, 37% 50UA 1.46A, 970mA -33DB, -33DB -45DBM -1.3DBM 28P 6.0x6.0x1.0MM - SKYWORKS SOLUTIONS INC.	
6	C308, C310	Inductor, Multilayer, Chip	ELCH0004710	1005GC2T15NJLF 15NH 5% - 250mA 0.53OHM 2GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	
6	L307	Inductor, Multilayer, Chip	ELCH0001430	LL1005-FHLR10J 100NH 5% - 150mA 2.2OHM 1.03GHZ 10 SHIELD NONE 1.0X0.5X0.5MM R/TP TOKO, INC.	
6	C333	Capacitor, Ceramic, Chip	ECCH0000701	C1005C0G1H1R2CT000F 1.2pF 0.25PF 50V NP0 - 55TO+125C 1005 R/TP - TDK CORPORATION	
6	CN201	Connector, Terminal Block	ENZY0028201	KQ03LT-3R 3P 2.50MM STRAIGHT SMD R/TP - HIROSE KOREA CO., LTD	
6	X101	Crystal	EXXY0018701	FC-135(12.5PF, +-20PPM) 32.768KHZ 20PPM 12.5PF 32*15 SMD R/TP SEIKO EPSON CORP	
6	FB203	Filter, Bead	SFBH0007101	BLM15AG121SN1D 120 ohm 1.0X0.5X0.5 25% 0.25 ohm 0.5A SMD R/TP 2P 0 MURATA MANUFACTURING CO., LTD.	
6	C336	Capacitor, Ceramic, Chip	ECCH0003002	C2012Y5V1A106ZT000N 10uF -20TO+80% 10V Y5V - 30TO+85C 2012 R/TP - TDK CORPORATION	
6	R310	Resistor, Chip	ERHZ0000423	MCR01MZIP5J154 150KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	L101	Inductor, Multilayer, Chip	ELCH0001431	LL1005-FHL68NJ 68NH 5% - 180mA 1.7OHM 1.3GHZ 10 SHIELD NONE 1.0X0.5X0.5MM R/TP TOKO, INC.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
6	C242	Capacitor, Ceramic, Chip	ECCH0042301	CL10A225KA5LNNC 0.0000022F 10% 25V X5R - 55TO+85C 1608 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	U300	IC, Bluetooth	EUSY0418701	BCM2070B2KUBXG 2.3VTO5.5V 158.4mW 42P - WLPGA R/TP 42P BROADCOM ASIA DISTRIBUTION PTE LTD	
6	R106	Resistor, Chip	ERHZ0000499	MCR01MZP5J562 5.6KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	X100	Crystal	EXXY0027001	DSX321G-26M(8PF) 26MHZ 10PPM 0F NONE SMD R/TP DAISHINKU CORPORATION.	
6	C122, C257, C354	Capacitor, Ceramic, Chip	ECZH0001210	C1005Y5V1A474ZT000F 470nF -20TO+80% 10V Y5V -30TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	R304	Resistor, Chip	ERHY0000128	MCR01MZP5F1502 15KOHM 1% 1/16W 1005 R/TP - ROHM.	
6	L309	Resistor, Chip	ERHZ0000441	MCR01MZP5J220 22OHM 5% 1/16W 1005 R/TP - ROHM.	
6	C208, C209, C233	Capacitor, Ceramic, Chip	ECCH0002001	C1005JB0J104KT000F 0.1uF 10% 6.3V Y5P - 30TO+85C 1005 R/TP - TDK CORPORATION	
6	FL301	Filter, Ceramic	SFCY0000901	LFB212G45SG8A166 BPF 2.45KHZ 100Hz SMD R/TP 4P MURATA MANUFACTURING CO., LTD.	
6	C235	Capacitor, TA, Conformal	ECTH0002703	TCTAL1A107M8R 0.0001F 20% 10V 50UA - 55TO+125C 0OHM 3.2x1.6x1.1 NONE SMD R/TP ROHM CO., LTD.	
6	L302	Inductor, Multilayer, Chip	ELCH0003838	LQG15HS8N2J02D 8.2NH 5% - 300mA 0.24OHM 3.7GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO., LTD.	
6	L201, L202	Inductor, Multilayer, Chip	ELCH0001404	LL1005-FHL1N5S 1.5NH 0.3NH - 400mA 0.13OHM 15GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TOKO, INC.	
6	L100	Inductor, Wire Wound, chip	ELCP0009410	LQM2HPN3R3MG0 LQM2HPN3R3MG0, 3.3 uH, N, 2x2.5x1.0, R/TP, chip power MURATA MANUFACTURING CO., LTD.	
6	CN300	Connector, BtoB	ENBY0042701	GB042-54S-H10 54P 0.4MM STRAIGHT SOCKET SMD R/TP 1M - LS Mtron Ltd.	
6	J200	Card Socket	EAG63032601	KCN-ET-0-0108 SIM 6P STRAIGHT SMD R/TP - KSD CO., LTD	
6	FB100	Filter, Bead	SFBH0007103	BLM15BB750SN1D 75 ohm 1.0X0.5X0.5 25% 0.4 ohm 0.3A SMD R/TP 2P 0 MURATA MANUFACTURING CO., LTD.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	PartNumber	Spec	Remark
6	R115	Resistor, Chip	ERHZ0002401	RC1005J123CS 12KOHM 5% 1/16W 1005 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	C116, C129	Capacitor, Ceramic, Chip	ECCH0000151	CL05B472KB5NNNC 4.7nF 10% 25V X7R - 55TO+125C 1005 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	CN202	Socket, Card	ENSY0023802	SCHB1B0201 Micro-SD 8P ANGLE SMD R/TP - ALPS ELECTRIC KOREA CO., LTD.	
6	R125	Resistor, Chip	ERHY0003301	MCR01MZP5J101 100OHM 5% 1/16W 1005 R/TP - ROHM.	
6	CN203	Connector, I/O	ENRY0008801	GU073-5P-SD-E1500 GU073-5P-SD-E1500, 5, mm, ANGLE LS Mtron Ltd.	
6	R214, R303	Resistor, Chip	ERHZ0000404	MCR01MZP5J102 1KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	SW300	Connector, RF	ENWY0007601	NMS-306 NMS-306, SMD, dB NMAE ELECTRONICS INC	
6	PT100	Thermistor, NTC	SETY0006301	NCP15XH103J03RC 10KOHM 5% 0V 0A 3.35KK SMD P/TP 1005size MURATA MANUFACTURING CO., LTD.	
6	L310	Inductor, Multilayer, Chip	ELCH0004707	1005GC2T1N5SLF 1.5NH 0.3NH - 300mA 0.13OHM 7GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	
6	L303	Inductor, Multilayer, Chip	ELCH0001049	1005GC2T6N8JLF 6.8NH 5% - 250mA 0.32OHM 3GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	
6	L306	Inductor, Multilayer, Chip	ELCH0004720	1005GC2T1N2SLF 1.2NH 0.3NH - 300mA 0.12OHM 9GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

12.3 Accessory

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	PartNumber	Spec	Remark
2	AFN053800	Manual Assembly, Operation	AFN75496104	LGA258.ACISTS ZZ:Without Color LGA258 manual assy for CIS	
3	MBM087200	Card, Warranty	MCDF0011303	COMPLEX GD350 CISBK ZZ:Without Color -	
3	MFL053800	Manual, Operation	MFL67214104	COMPLEX LGA258.ACISTS ZZ:Without Color LGA258 manual for CIS	
2	EAC00	Rechargeable Battery, Lithium Ion	EAC61679101	LGIP-430N-WWU-LGC PRISMATIC 3.7V 900AH 180AH 34x50x4.6 34.15x53x4.7 BLACK inner pack 463450, 900mAh, Innerpack, Up LG Chem, LTD.	
2	EAY060000	Adapters	SSAD0038301	100-240V, 5060 Hz, 5.1 V, 700 mA, CE, AC-DC Adaptor, 90Vac~264Vac, 5.1V, 700mA, 5060, WALL 2P, USB,	
2	MEZ002100	Label, Approval	MEZ63927701	COMPLEX LGP500.ACISBK ZZ:Without Color Label (Kazakhstan KST Mark)	
2	MEZ002101	Label, Approval	MEZ64188201	COMPLEX LGA190.ACISBK ZZ:Without Color -	
2	EBX000000	Accessory, Data Cable	SGDY0018001	LG0029 LG0029 Micro USB, 0.8M ningbo broad telecommunication co., ltd	